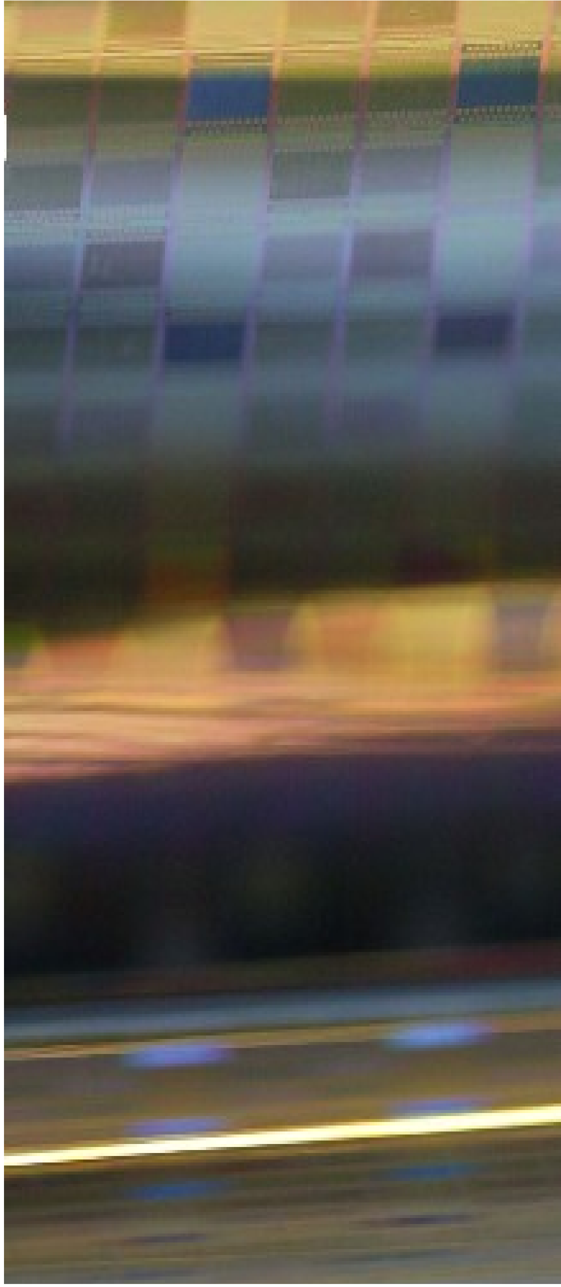
rication of Electronics on Flexible Substrate Using Self-Aligned Imprint Lithography (SAIL)



Ohseung Kwon, Marcia Almanza-Workman, Alison Chaiken, Warren Jackson, Albert Jeans, Han-Jun Kim, Hao Luo, Ping Mei, Craig Perlov, Carl Taussig

Hewlett-Packard Company, Palo Alto, CA

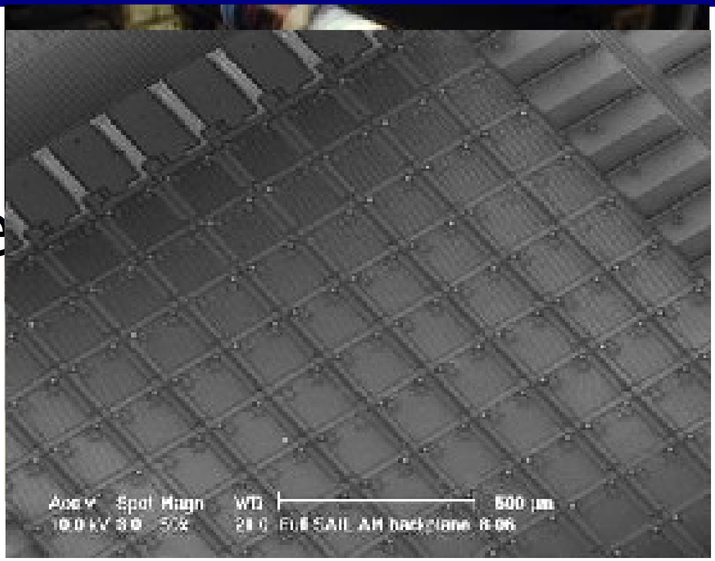
Frank Jeffrey, Steve Braymen, Jason Hauschildt

PowerFilm Solar Inc, Boone, IA

Overview

- Why SAIL?
- SAIL process modules:
  - Thin film deposition
  - Imprinting
  - Self-aligned etching
- SAIL flexible AM backplane
  - a-Si R2R TFTs & arrays on plastic substrate
- Conclusion

R2R processing is a key enabler
for high throughput, low cost production of large area, flexible electronics!



R2R fabricated SAIL TFT array

Why SAIL?

Objective: R2R flexible AM backplanes

- Large Area
- High Resolution
- Inexpensive

Advantages of SAIL

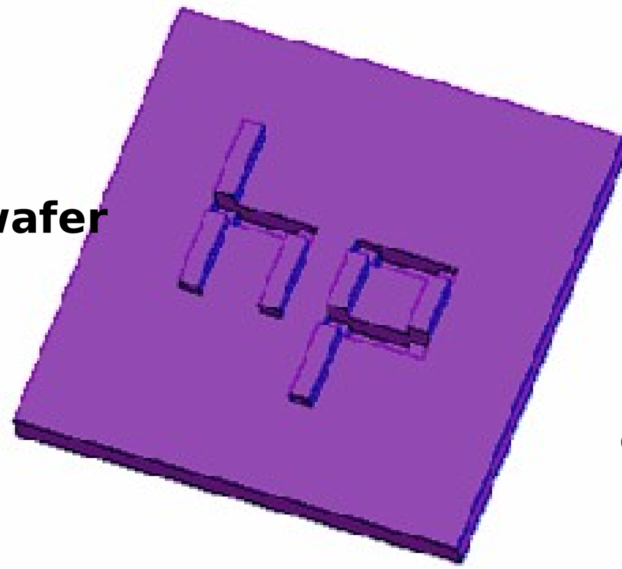
End-to-end R2R process
High Throughput, Enhanced Uniformity, Less Cleanroom Requirement

Sub-micron interlayer alignment on meter-scale substrates
Sub-micron Patterning Resolution, Faster Response Time

Opportunity for Lowest Possible Process Cost
No Photolithography during Production, Equipment Scaled with Width not Area

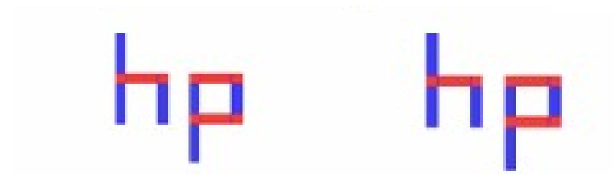
The Big Problem:
Patterning & Aligning on a Flexible Substrate

conventional alignment on wafer

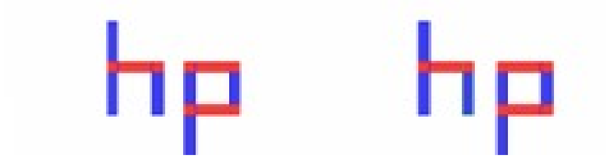


3D imprint mask combines multiple binary mask levels

alignment problem for web



Fix: do all masking in one step!



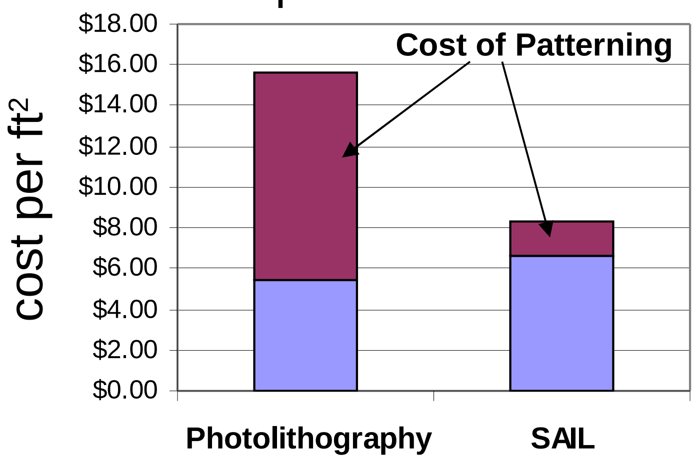
Imprint Lithography:
The Best Choice for R2R Patterning

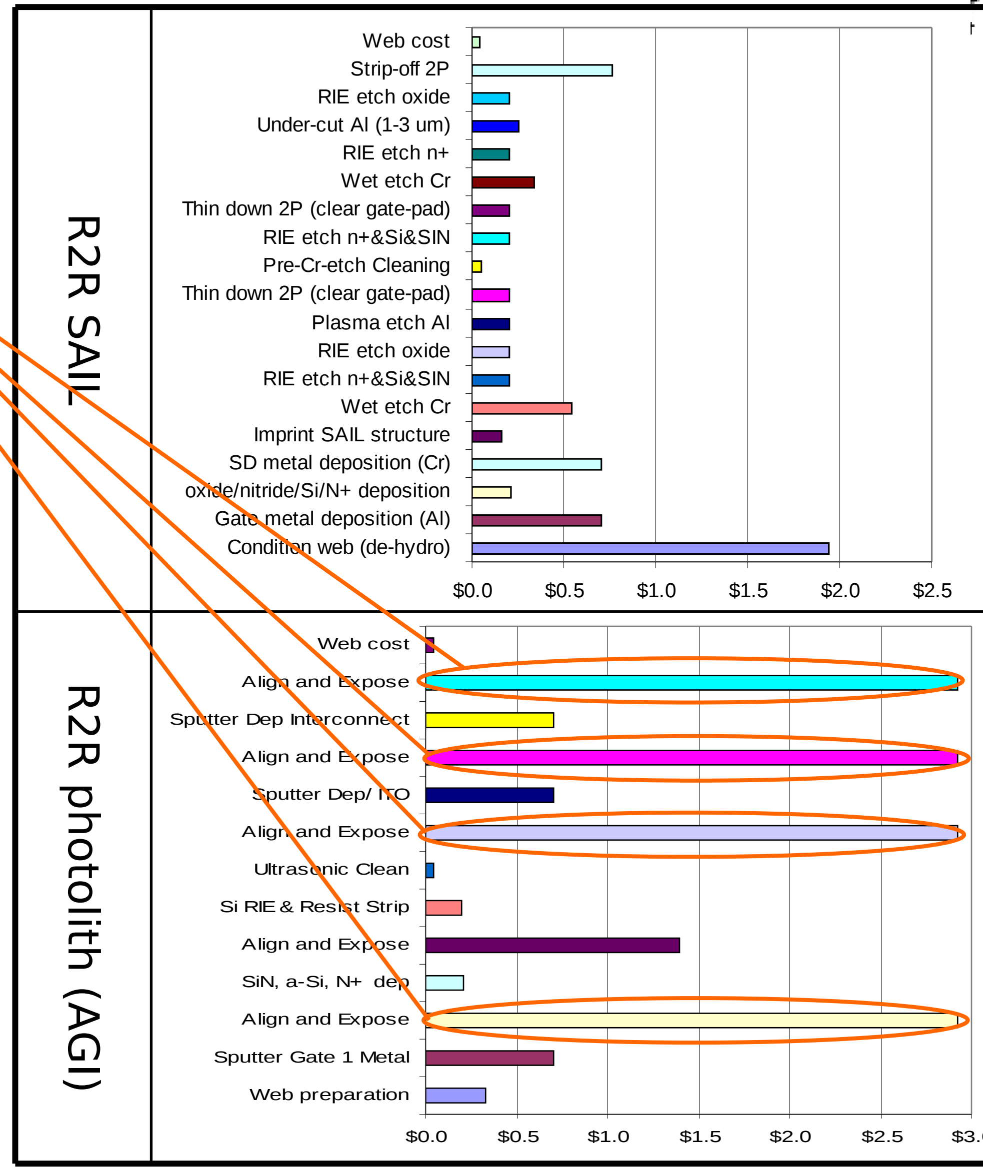
	photolithography	imprint lithography	inkjet
Throughput	moderate: limited by step & repeat / stitching	high: > 5 meters/min	low
Resolution	limited by substrate flatness ~10µ	100nm demonstrated	>10µ
Materials	PECVD Si, Si_3N_4, SiO_2, vacuum deposited metal, many others	PECVD Si, Si_3N_4, SiO_2, vacuum deposited metal, many others	must be jettable
Alignment of multiple levels	Difficult or Impossible due to web's dimensional instability	Self-alignment of multiple patterning layers	Requires secondary sensor

SAIL solves alignment problem & saves money

Multiple photoresist applications dominate photolithography process materials costs

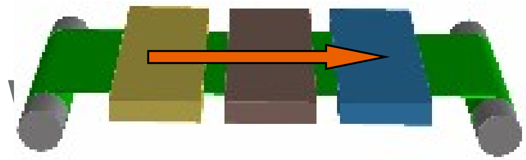
Backplane materials costs for R2R photolith & SAIL





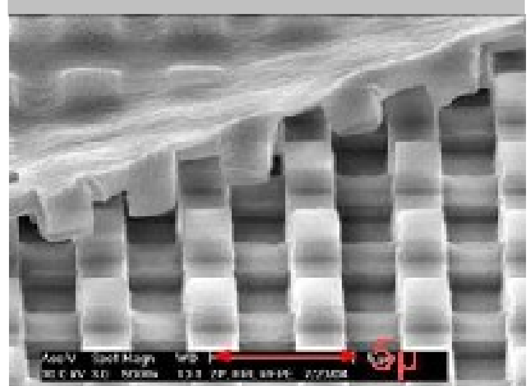
What is SAIL?

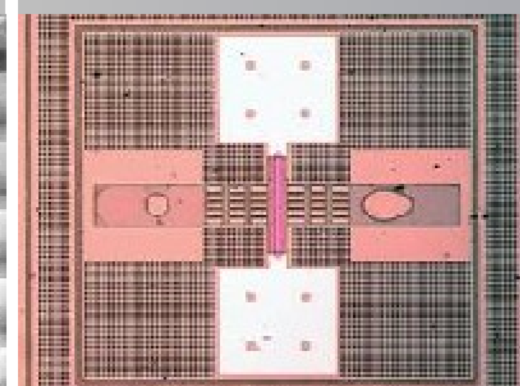
3 sequential processes on the flexible



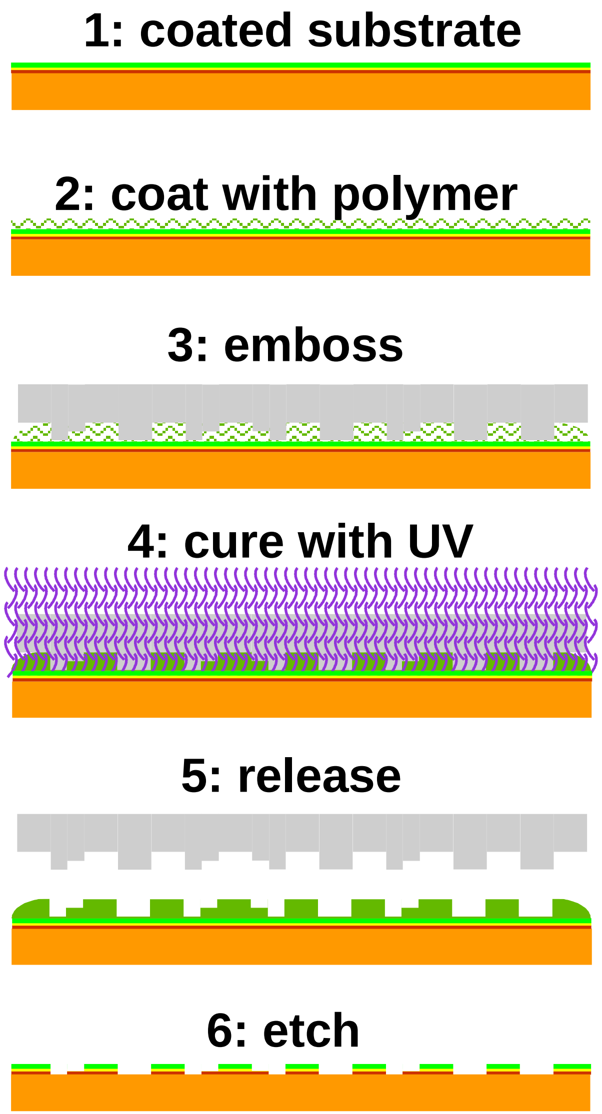
Deposition	Imprinting	Self-aligned etching
Vacuum deposition of metals, dielectrics, and semiconductors	Multiple mask levels imprinted as single 3-D structure	Patterning with wet and dry processes based on the imprint mask

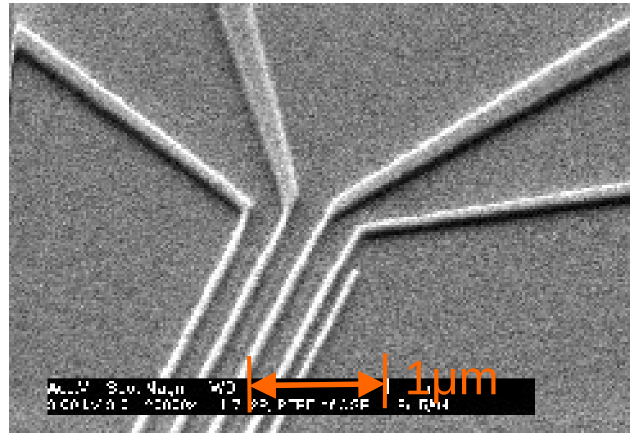
Fully R2R



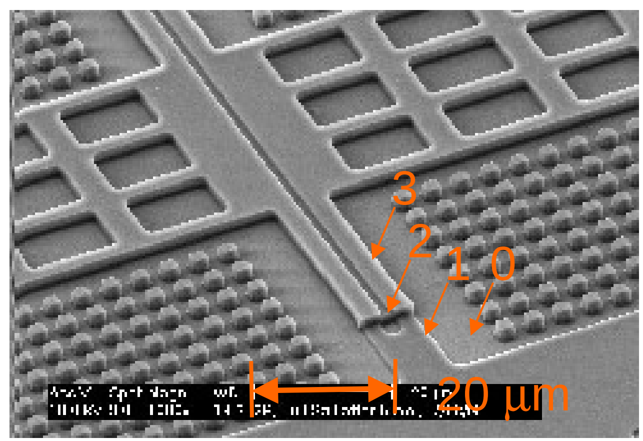


Basic Imprint Lithography Process





~40nm lines on 50µ polyimide



4 levels in 0.5 µ step heights

Pixel speed depends linearly on mobility but inversely with the square of channel length

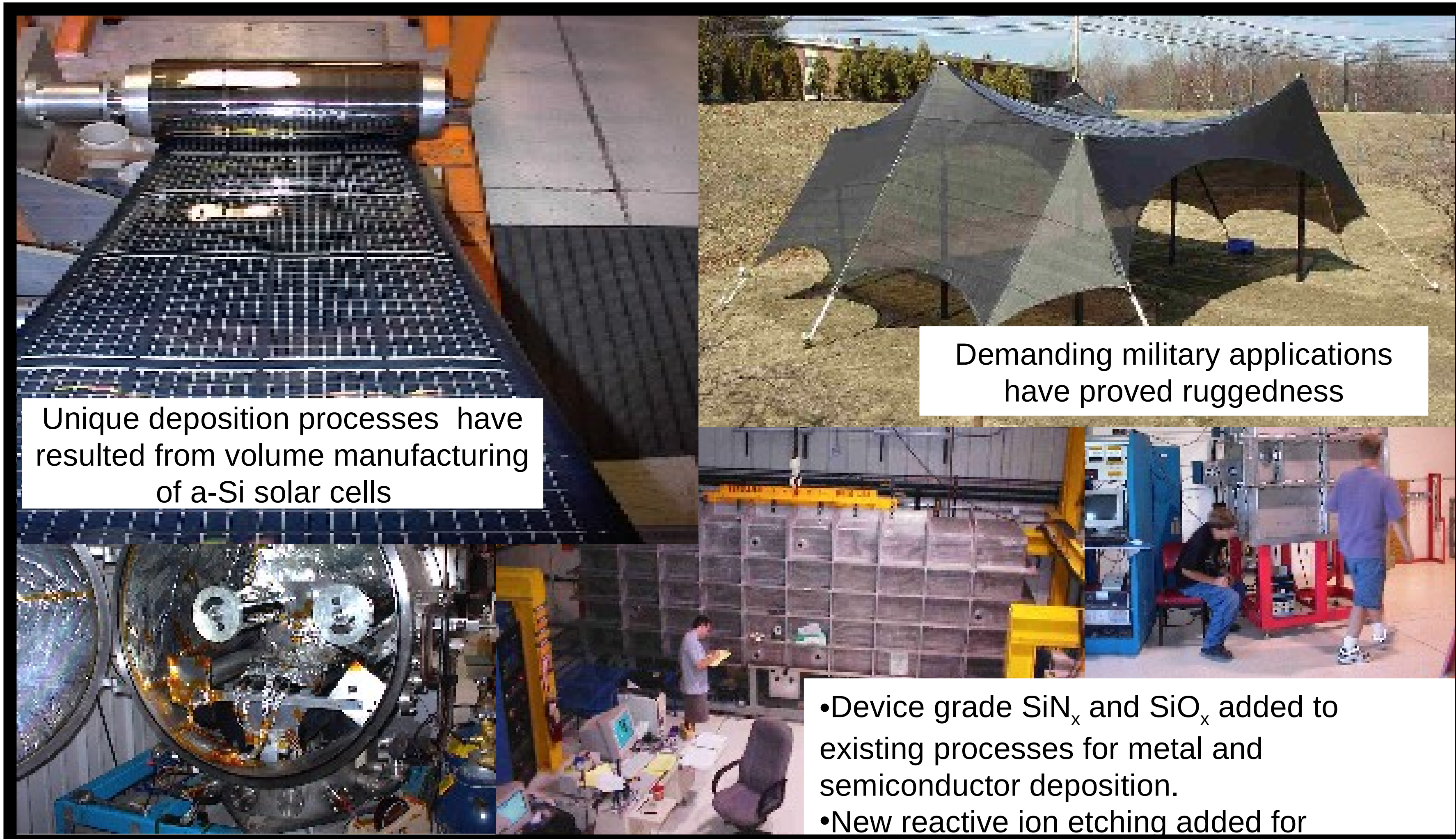
$$t_{pixel} \approx \frac{2\,L^2}{\mu\,(V_G - V_T)}$$

Multilevel structures on flex at 5m/min

Roll-to-Roll (R2R) Fabrication of Electronics

If you want lemonade;
start with lemons

SAIL process: Deposition

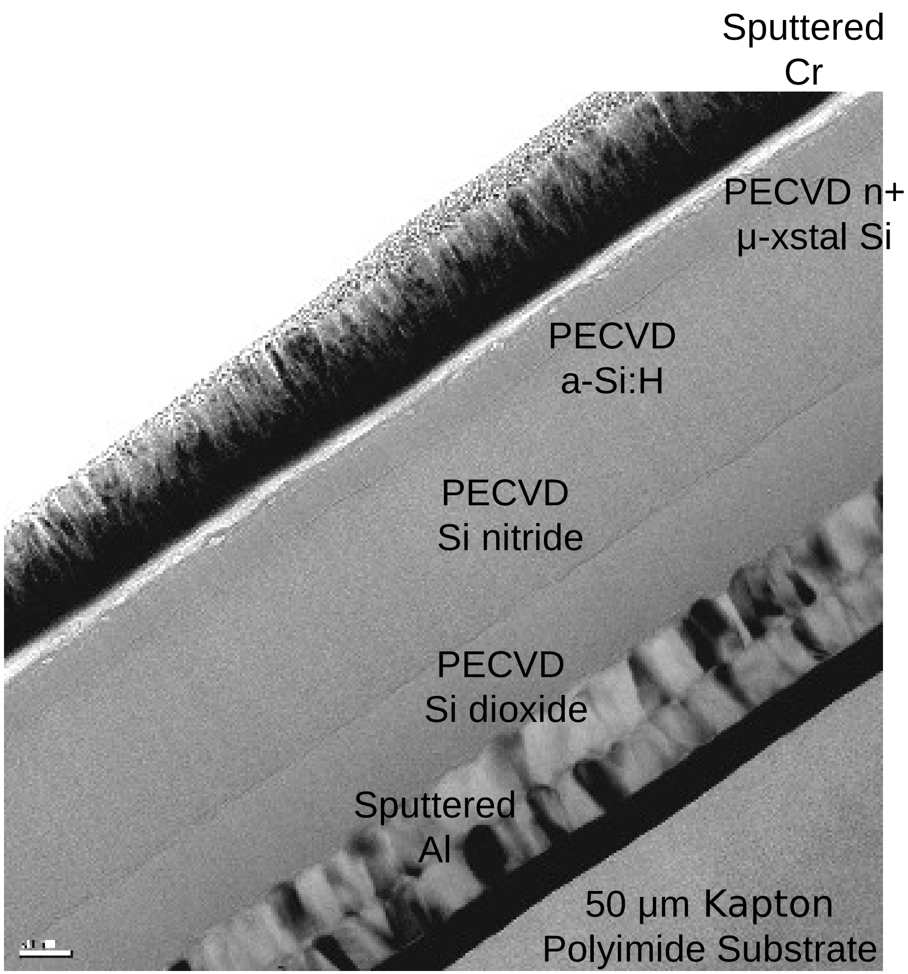


Unique deposition processes have resulted from volume manufacturing of a-Si solar cells

Demanding military applications have proved ruggedness

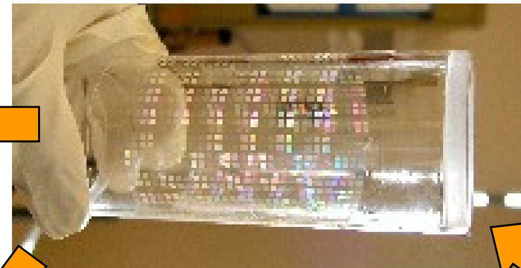
- Device grade SiN_x and SiO_x added to existing processes for metal and semiconductor deposition.
- New reactive ion etching added for patterning

SAIL process: Deposition

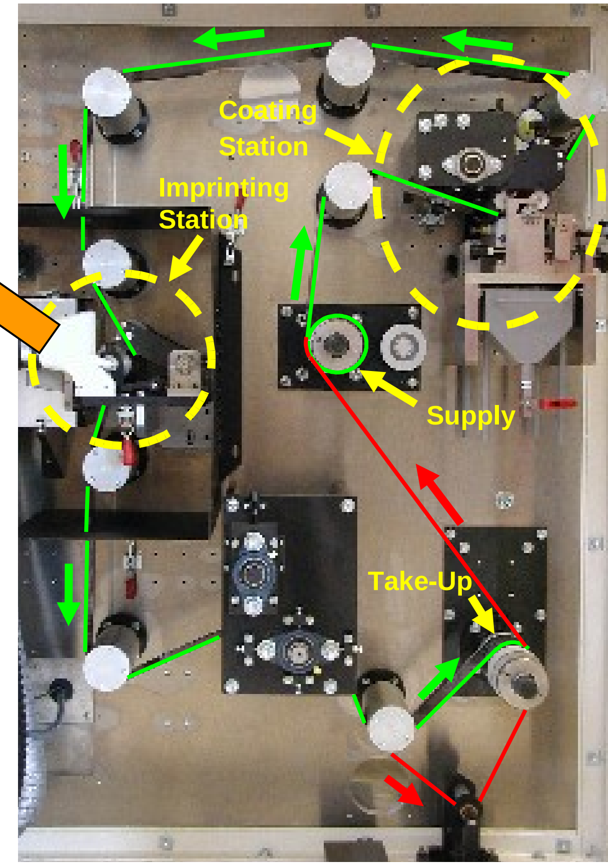


- R2R deposition requires different strategies for SiN_x/a-Si interface than batch process
- In-line uniformity enhances with R2R due to steady state process
- SAIL enables in-line deposition of full TFT stacks in the same vacuum chamber providing clean interfaces without expensive cleaning steps
- Taking advantage of the 1µm channel lengths provided by SAIL requires

SAIL process: Imprinting

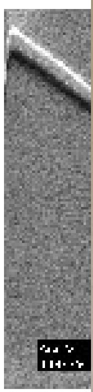


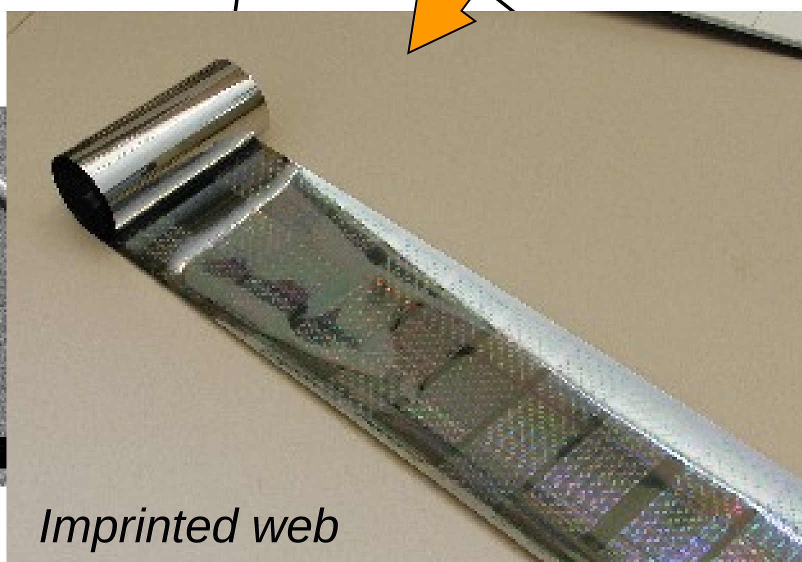
Imprinting roller with elastomeric stamp

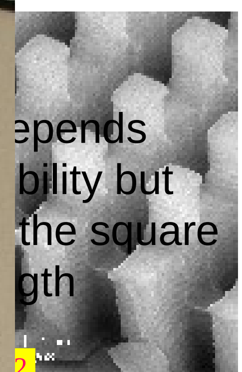


House-built R2R coating & imprinting machine

(Throughput rate = **5 m/min**)







epends
bility but
the square
gth

ct ratio
o heights
→ **sub-micron** features with
4 levels and **5:1 aspect ratio**

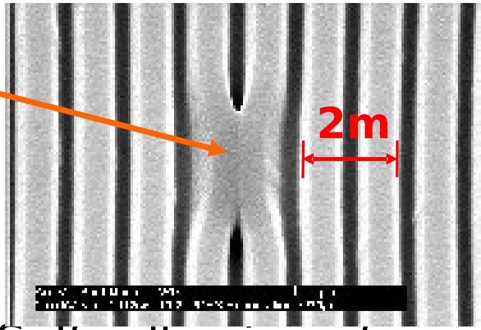
→ **40 nm** line width

R2R Imprint Technology: Stamp Life

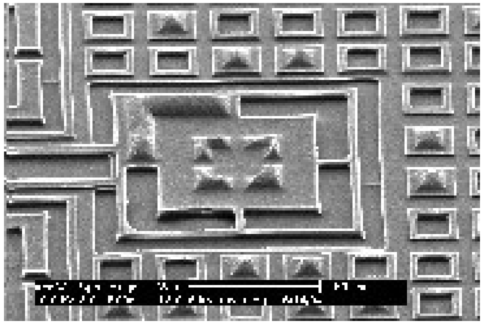
Typical R2R web length 1-2Km requires 1-2K impressions from a 1m stamp

Failure modes

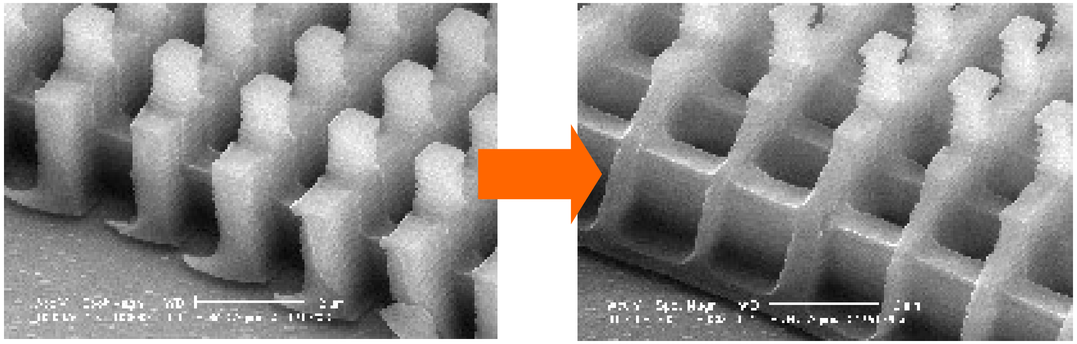
- Pairing: adhesions between closely spaced features
- Swelling: solvent transfer from photopolymer to stamp
    - CD loss
    - 'lock-in' and breakage



Self-adhesion of stamp

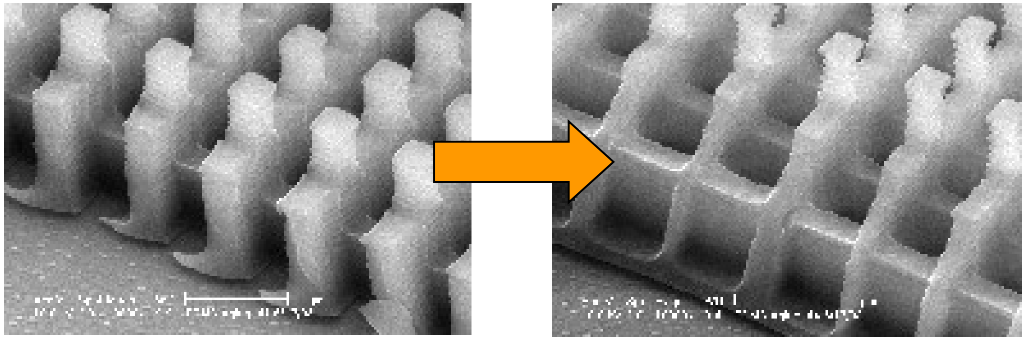


stamp fragment embedded in imprinted polymer



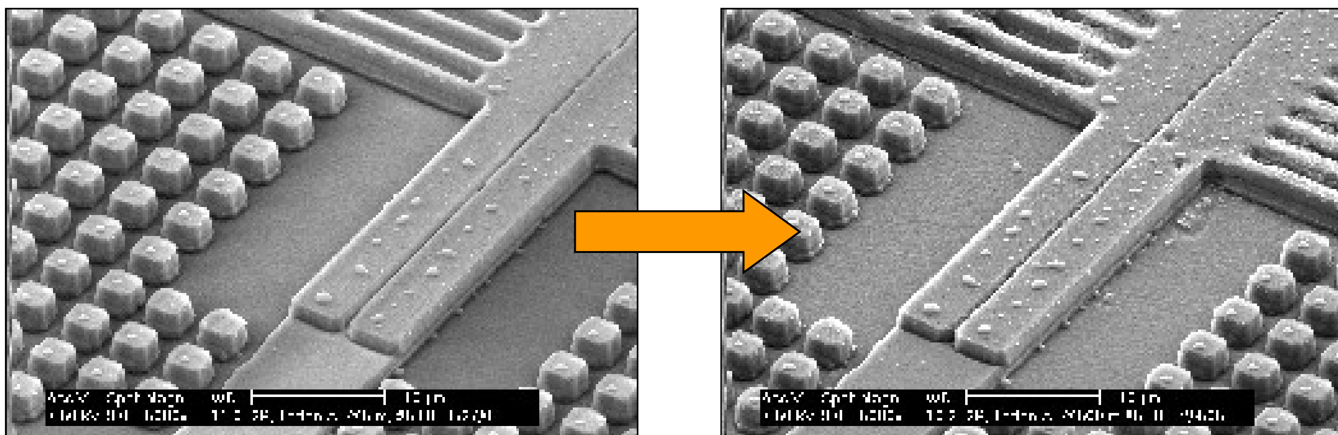
Loss of feature critical dimension due to stamp swelling after only 40 impressions

Towards longer stamp life



Loss of feature critical dimension due to stamp swelling after only 40 impressions

Now, R2R coating and printing steps have reached a mature stage.



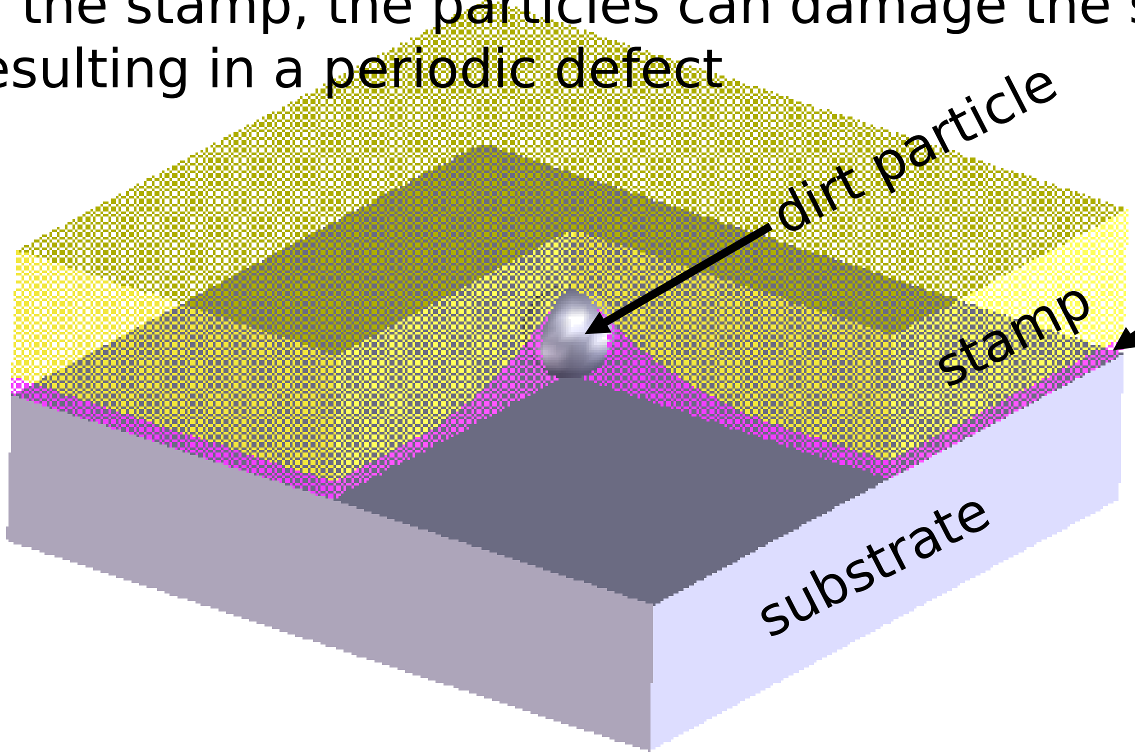
Impressions in photopolymer from fluorocarbon stamp when new (left) and after 2500 impressions (right)

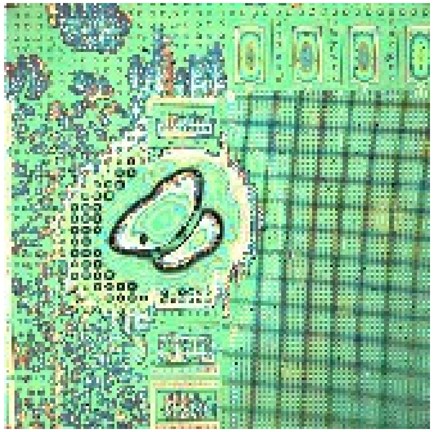
R2R Imprint Technology: stamp material screening tests

Material	Pairing, 1 µm pitch lines	Air Permeability (cm^3(STP) / cm. sec. cm Hg)	Swelling Test, Acetone	Resolution, 40 nm lines
Stamp Material A	Poor	28e-9 (est.)	5.5%	Poor
Stamp Material A	Good	28e-9 (est.)	Not tested	Poor
Stamp Material C	Excellent	13e-9	<0.5%	Fair
Stamp Material D	Not tested	Unknown	2.0%	Good

Affects of Particulate Contamination on the Imprinting Process

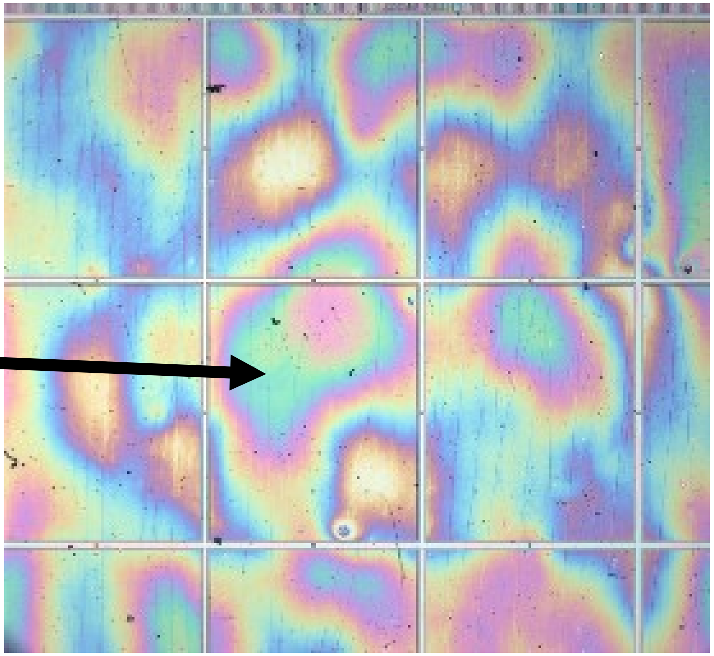
- particle lifts the stamp off of the substrate forming a 'tent' which disturbs the pattern for several diameters.
- although we do not observe particles embedded in the stamp, the particles can damage the stamp resulting in a periodic defect

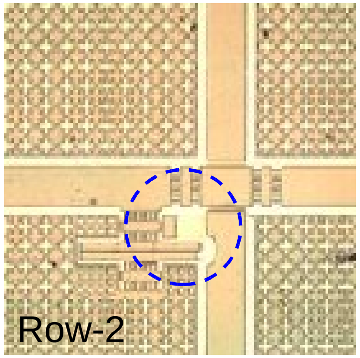


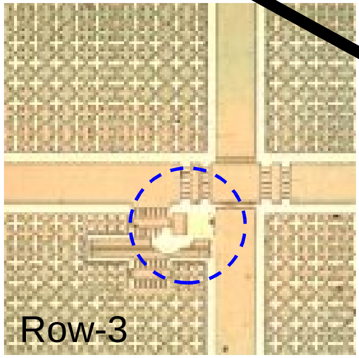


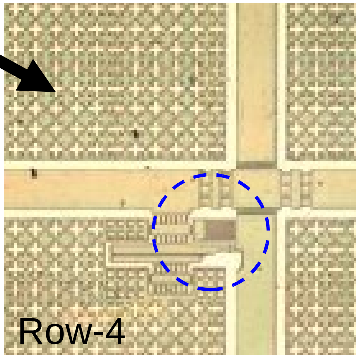
Non-uniformity in imprint process:

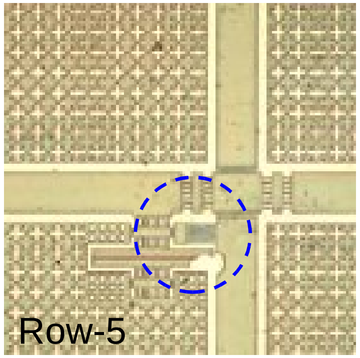
Type of nonuniformity	Description	Examples of sources
Non-repeatable	Not periodic, uncorrelated with pattern	Coating problems
Non-pattern dependent repeatable	Periodic but does not depend on stamp geometry	Roller or stamp roughness
Pattern dependent	Depends on features of stamp	Layout errors, master step height mismatch





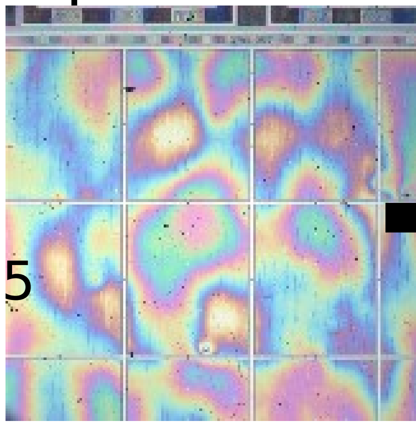


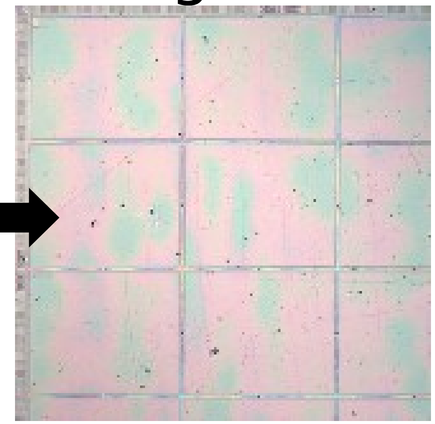




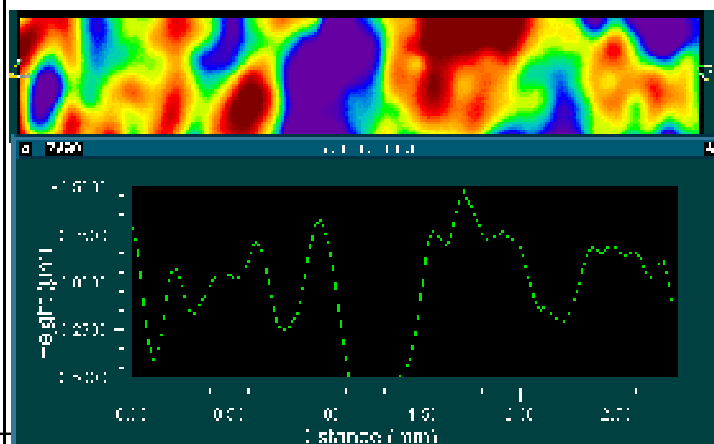
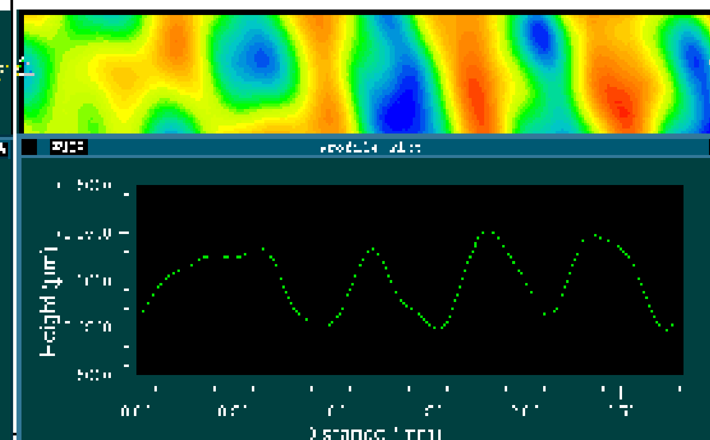
Smoothness of quartz and backing roller critical

Imprint nonuniformity before over 0.5 µ





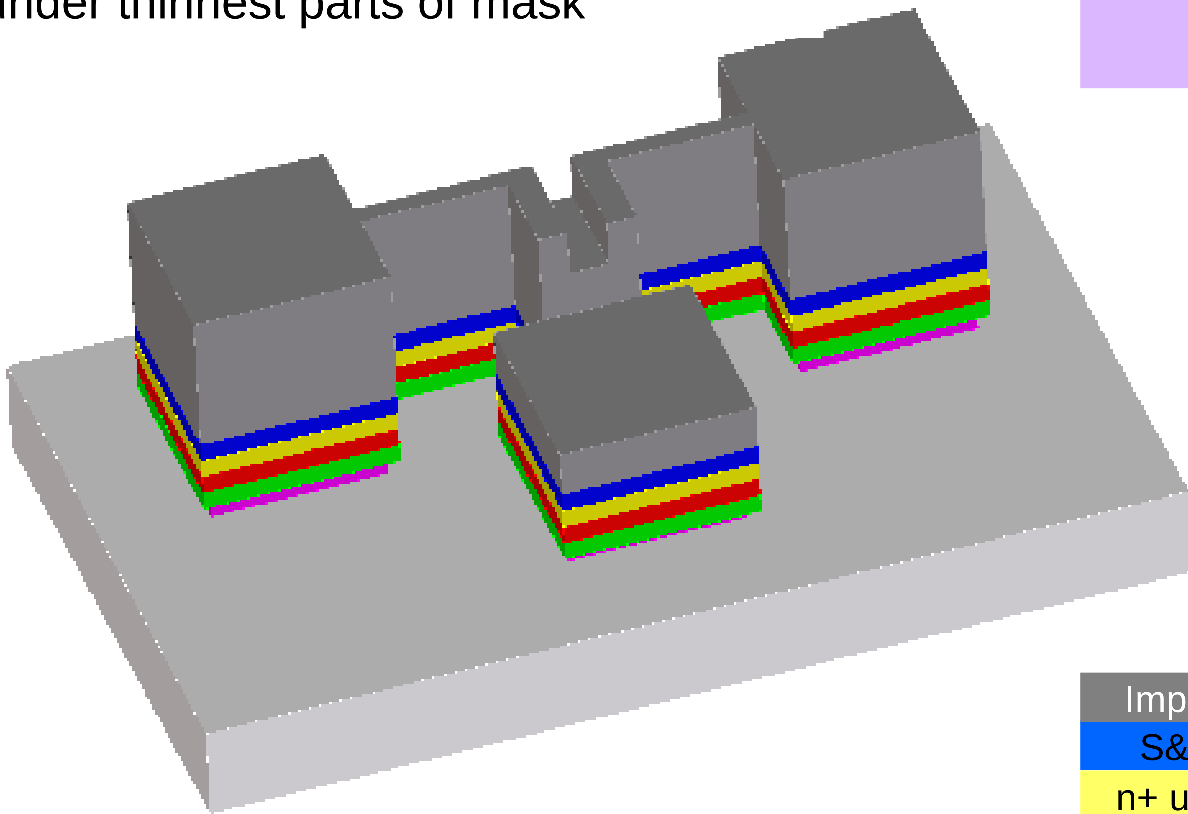
Current imprint nonuniformity approx. 0.1 µ

	Before	After
Quartz roller		
Rubber roller		

SAIL process: Etching

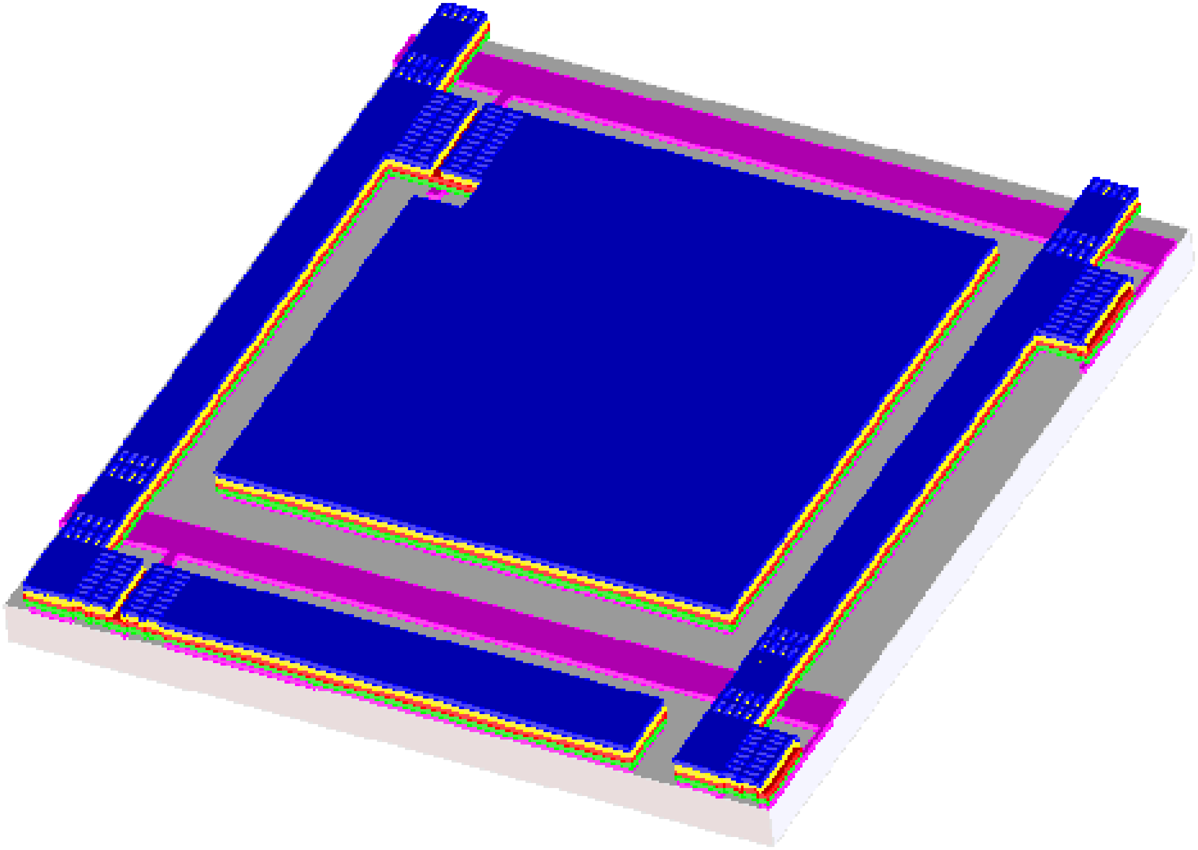
Then undercut to remove from under thinnest parts of mask

Individual SAIL TFT device



Imprint polymer
S&D metal Cr
n+ uC Si contact
a-Si semiconductor
SiNx dielectric
Gate metal Al
Polymer substrate

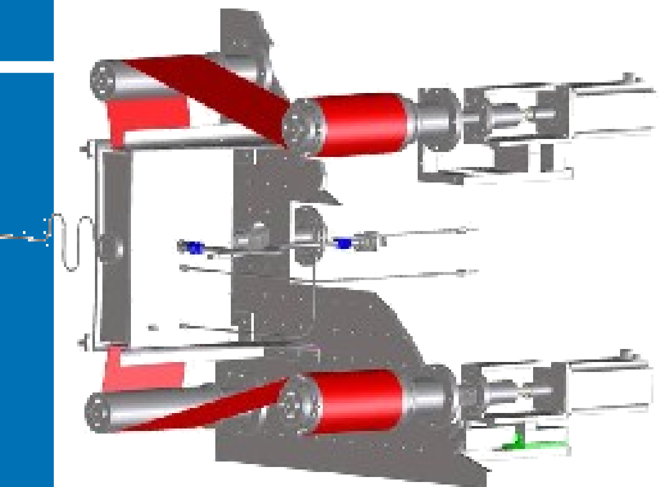
SAIL process: Etching

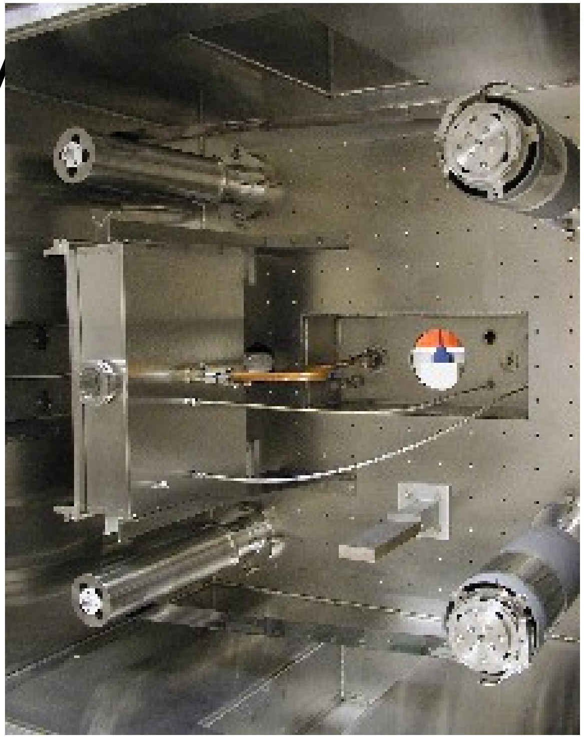


Remove remaining polymer to expose completed backplane

Unit cell in SAIL TFT array

R2R Plasma Etching Technology





Requirements
- Uniformity: process margin
- Anisotropy: minimize CD loss in etch mask

Challenges
- Batch endpoint detection methods won’t work for a stationary R2R process
- Achieving anisotropy with a grounded web is difficult

R2R Etch Endpoint Detection and Control

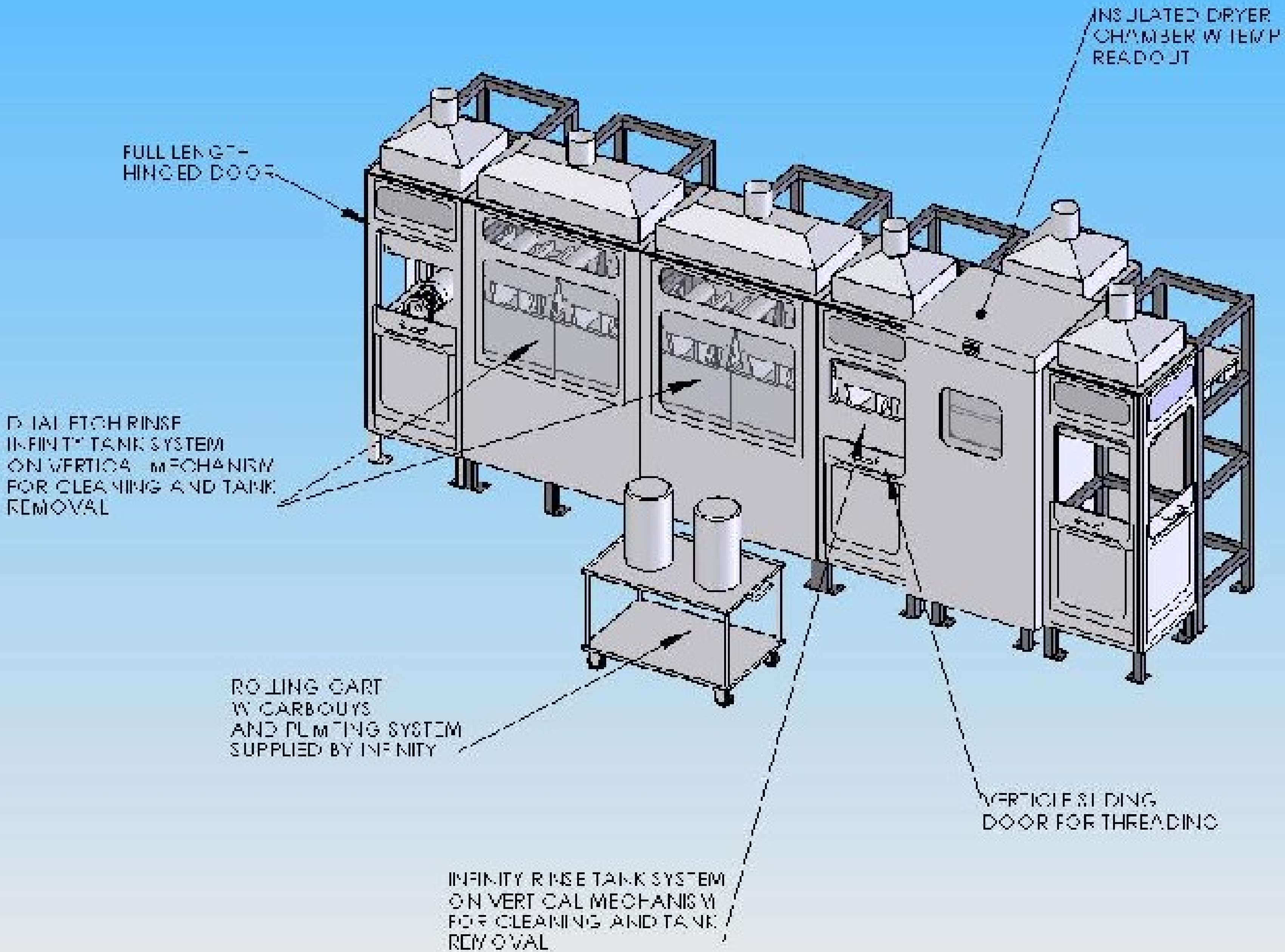
Requirements for detection
•Must work for steady state process
•Non-contact
•Vacuum compatible
•'Analog' output for etching polymer

Detection candidates (Optical)
•Fluorescent dye for polymer etch
•Reflectometry for thin films

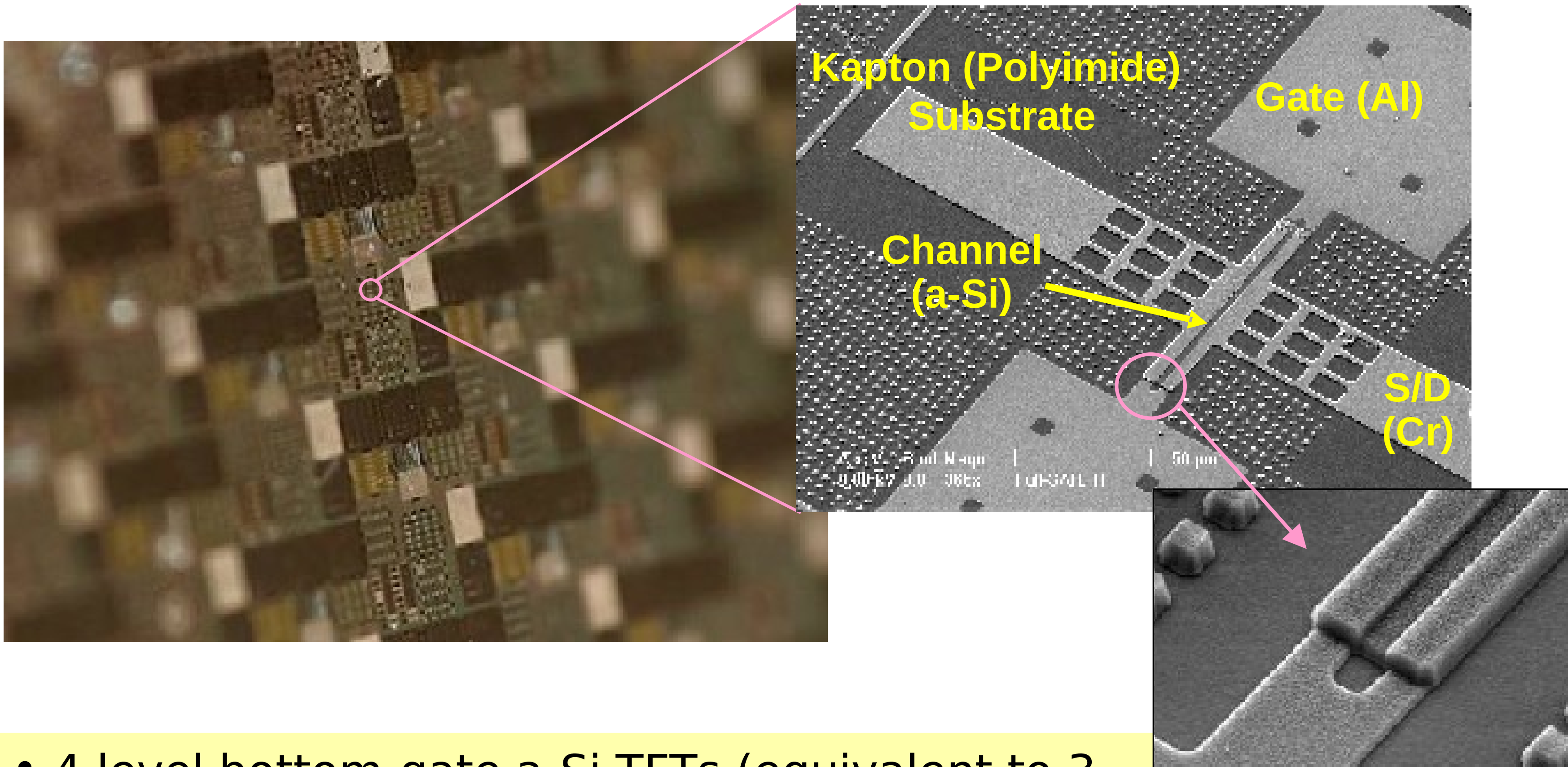
Control options
•Plasma power
•Flow rate composition
•Web speed

Coaxial fiber optic reflectometry probe in ITFT's R2R RIE. Measurement made on tangent section of web just after exiting roller

Wet R2R Etcher

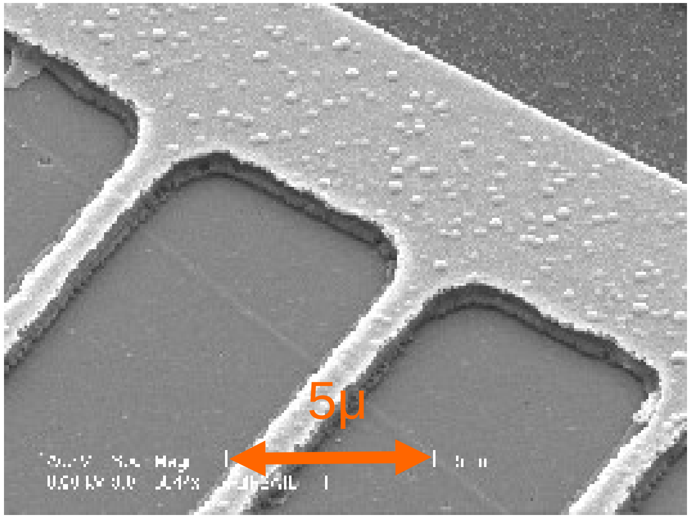


SAIL TFTs

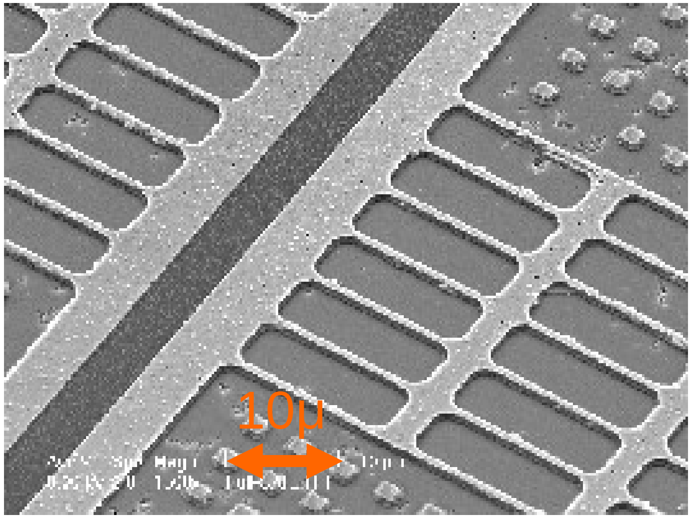


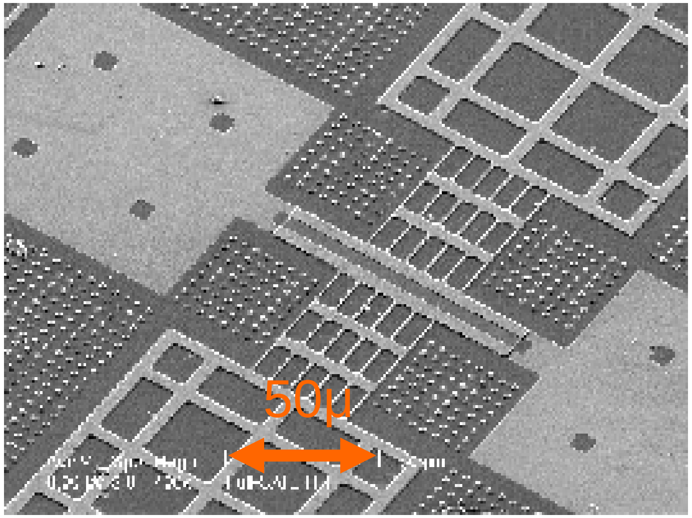
- 4 level bottom-gate a-Si TFTs (equivalent to 3 masks)
- Deposition, imprinting and dry etching with R2R
- S/D areas are separated from the gate area by wet etching

SAIL backplane: array ‘unit cell’ TFT

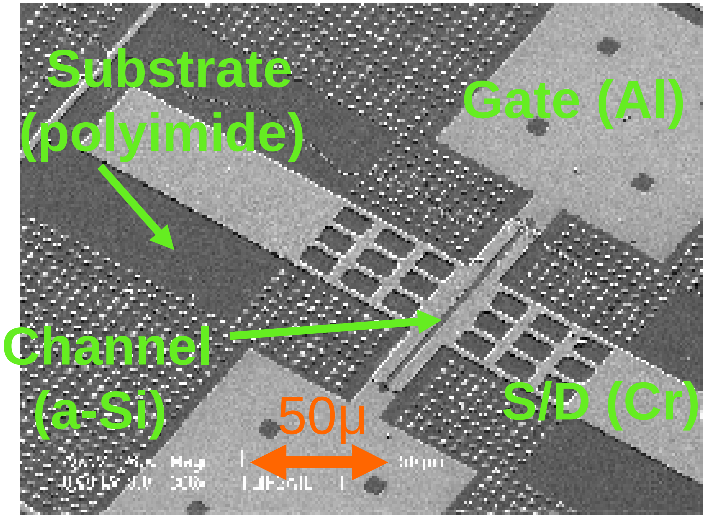


Undercut etch patterns bottom metal to isolate gate contact beneath S/D metal

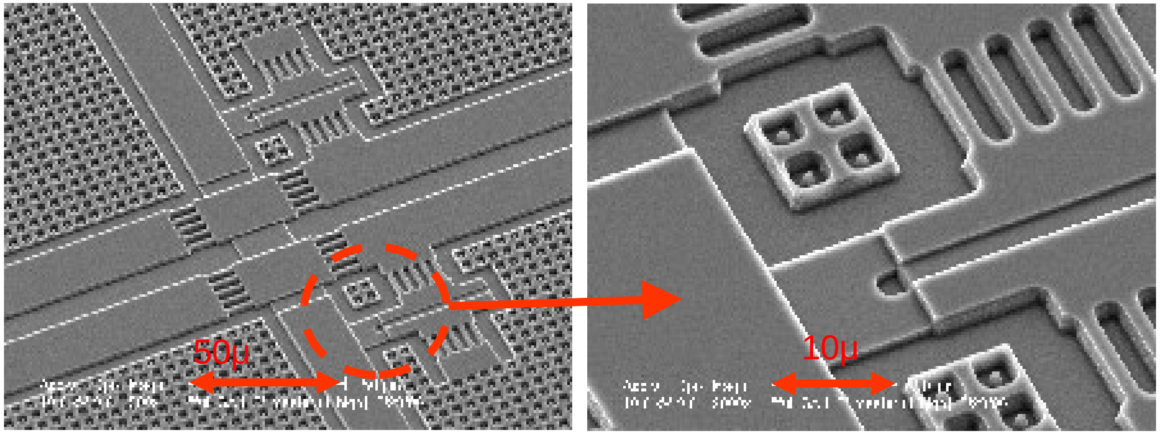




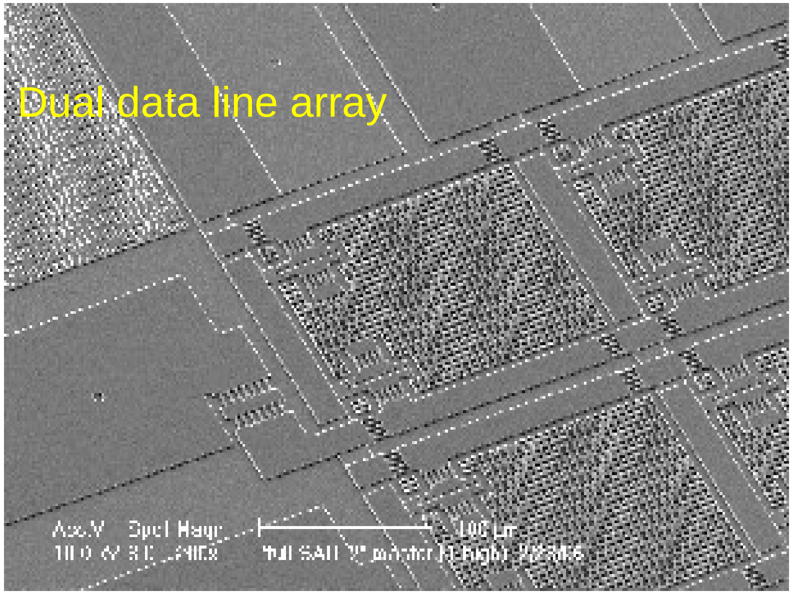
Perfect alignment maintained throughout 30m long web



SAIL backplane

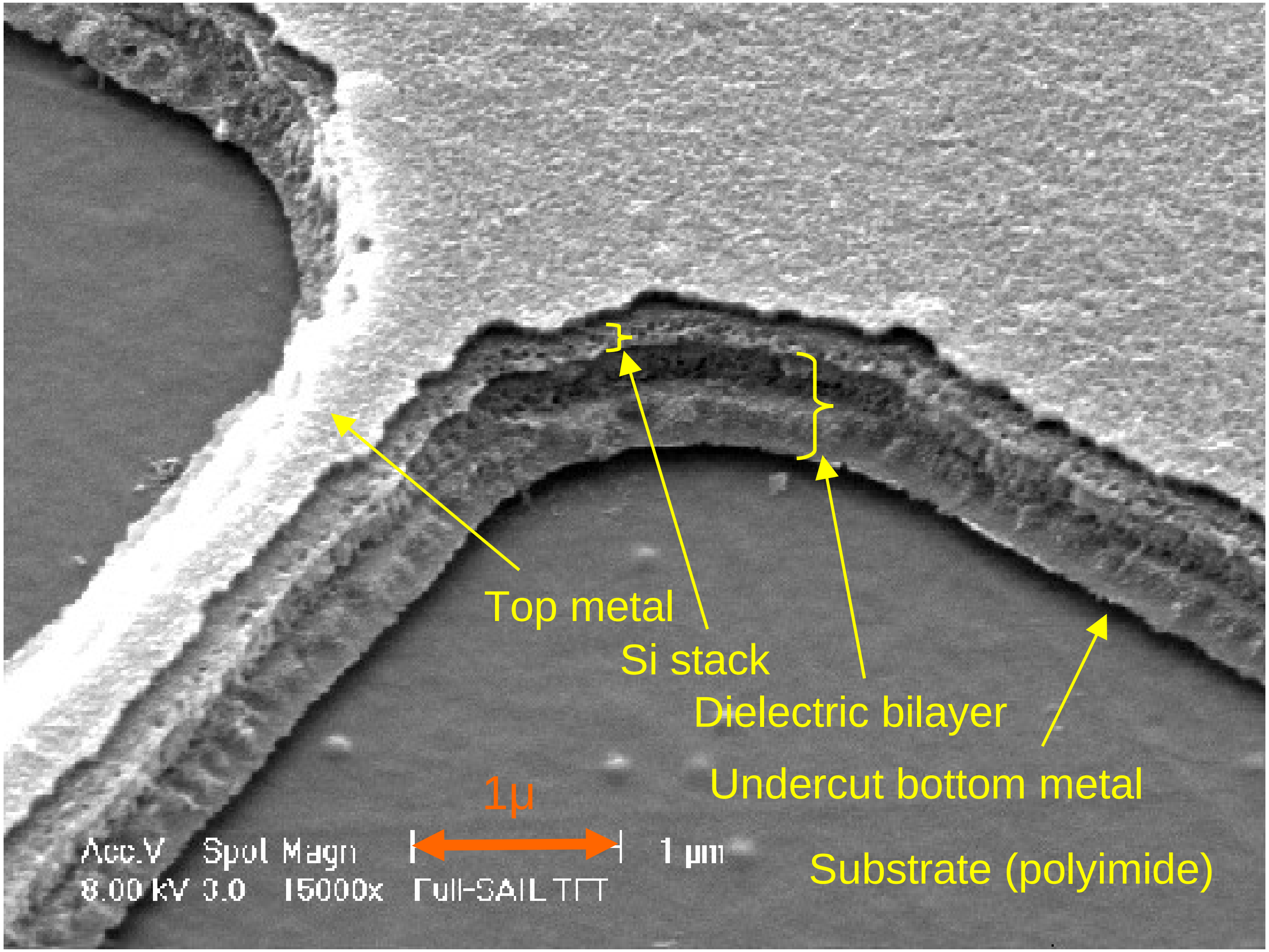


- 4 level mask
- W/L = 40/2µ TFTs

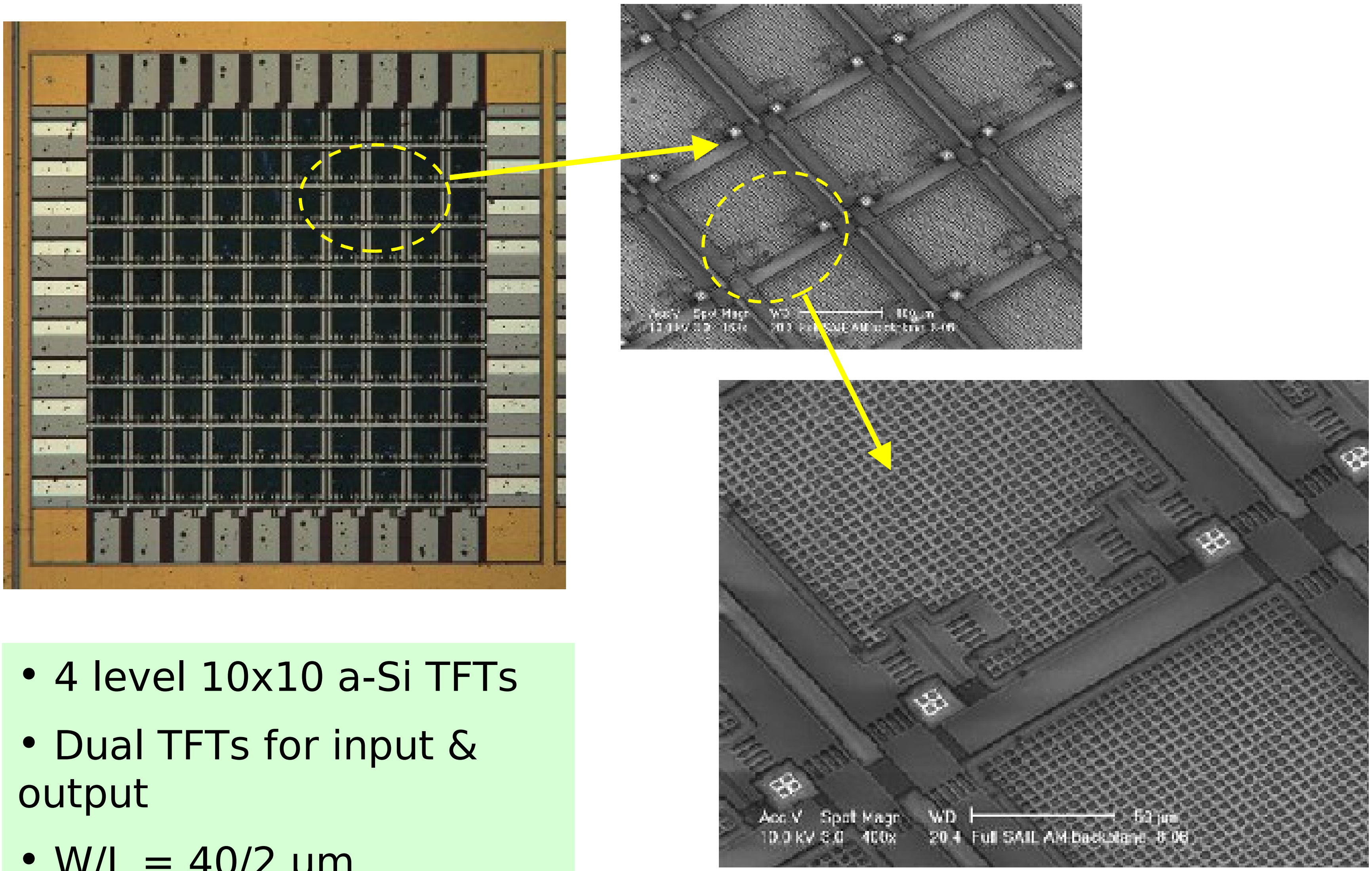


Arrays designed with two separate data lines connected to each pixel for full testing on probe station with or without integration with front plane

SAIL backplane: array 'unit cell'
Undercut used to pattern bottom metal

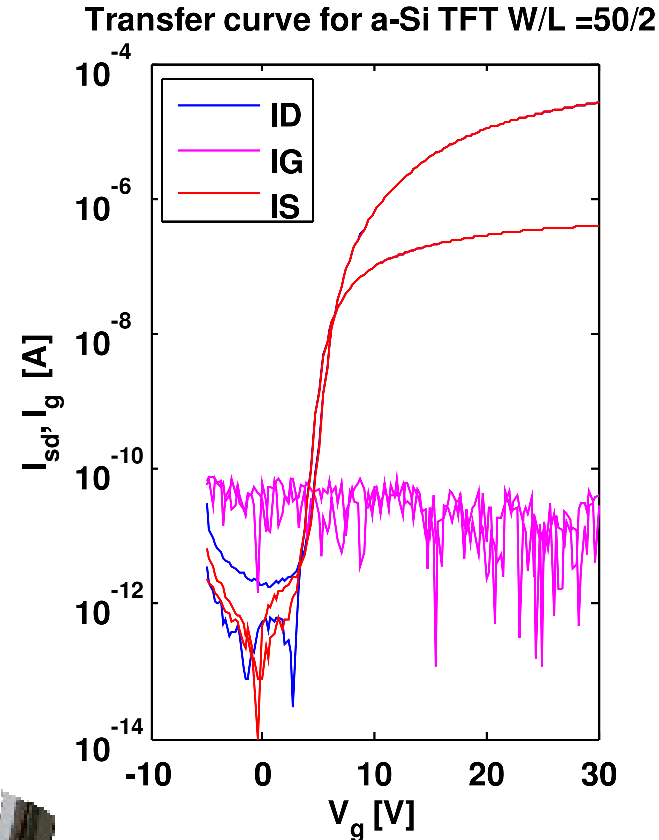


10x10 array AM backplane



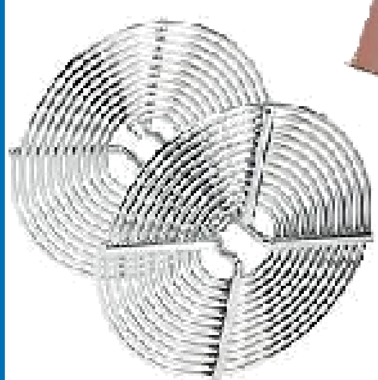
- 4 level 10x10 a-Si TFTs
- Dual TFTs for input & output
- W/L = 40/2 µm

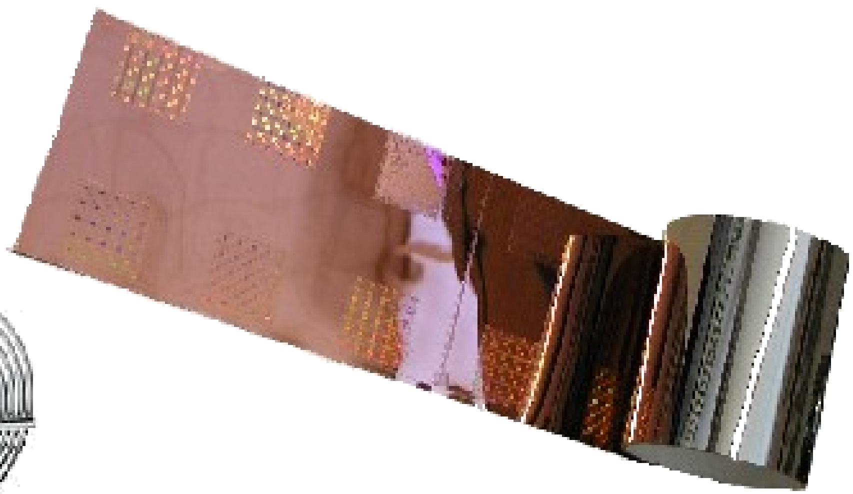
TFTs with Complete R2R Processing

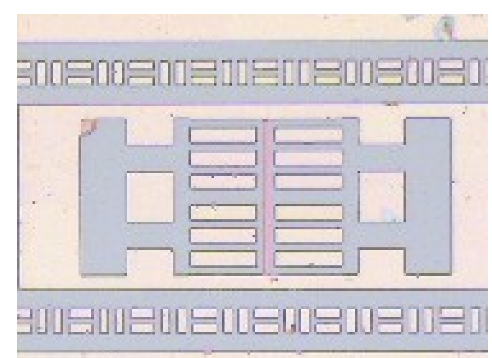


TFTs with un-patterned bottom gates

- R2R, deposition, imprinting, & dry etching
- R2R wet etch demonstrated but current process performed on 4m long batches using modified film processing reels
- TFT performance equal or better to batch fabricated devices

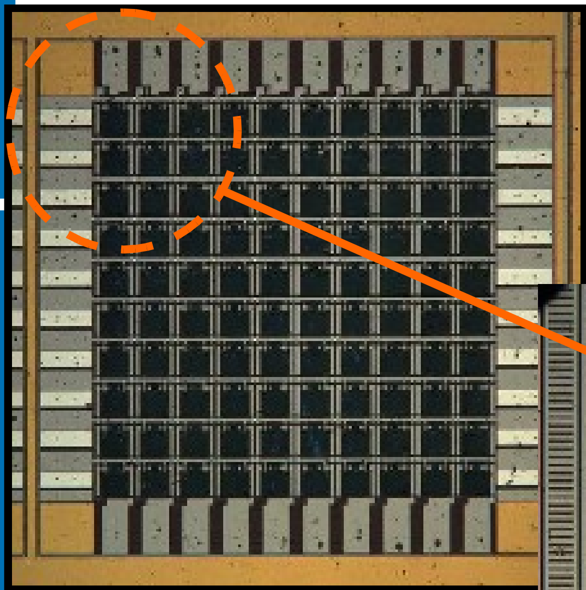


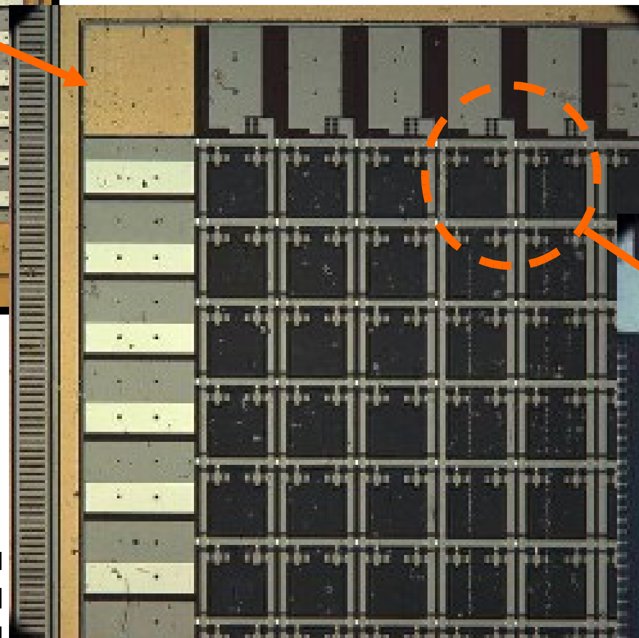


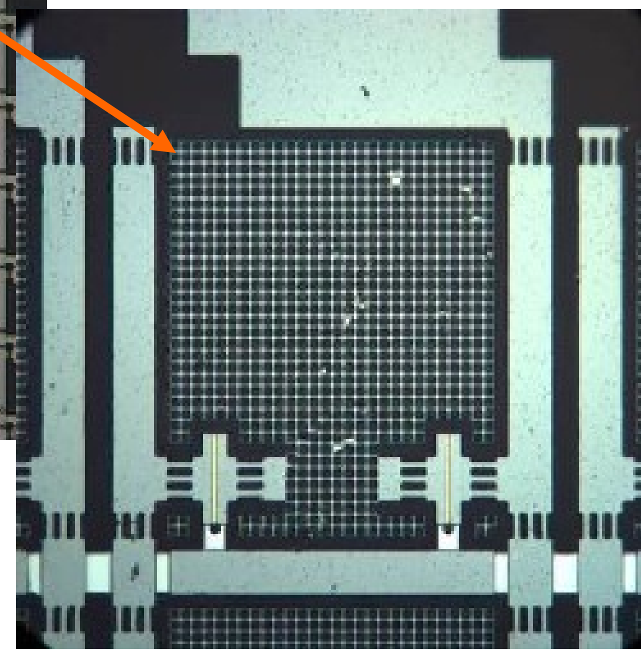


‘Full-SAIL’ TFT arrays:

complete active matrix with fully patterned gate lines

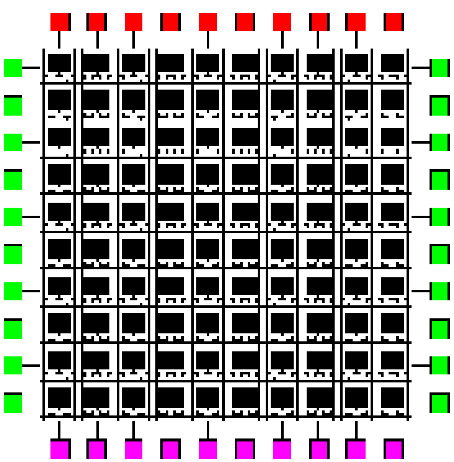






Input data lines

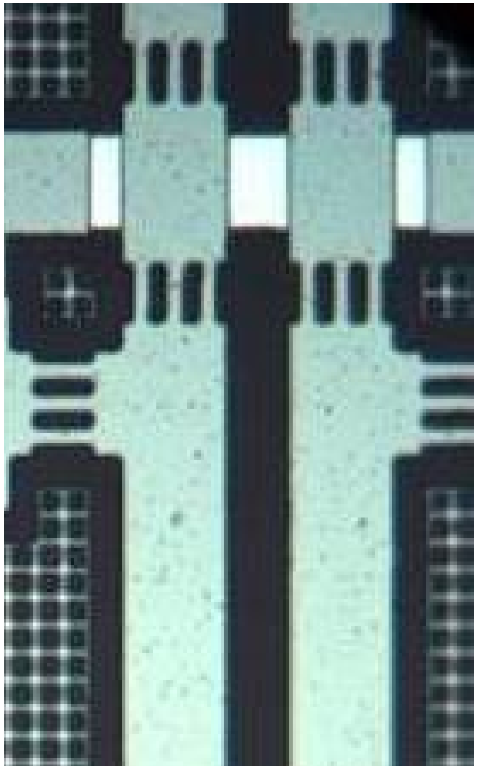
gate lines



Output data lines

2nd data line allows full electrical evaluation on probe station while still leaving array usable for integration with front plane

‘Full-SAIL’ TFT arrays:
undercut of bottom metal isolates gate lines



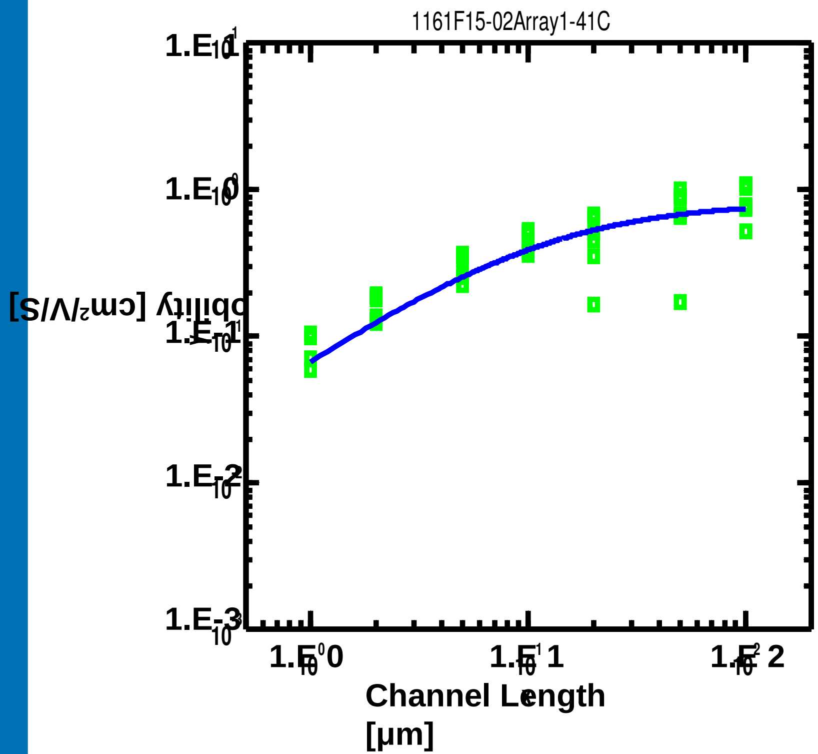
Fully processed array showing crossover of gate lines by data lines

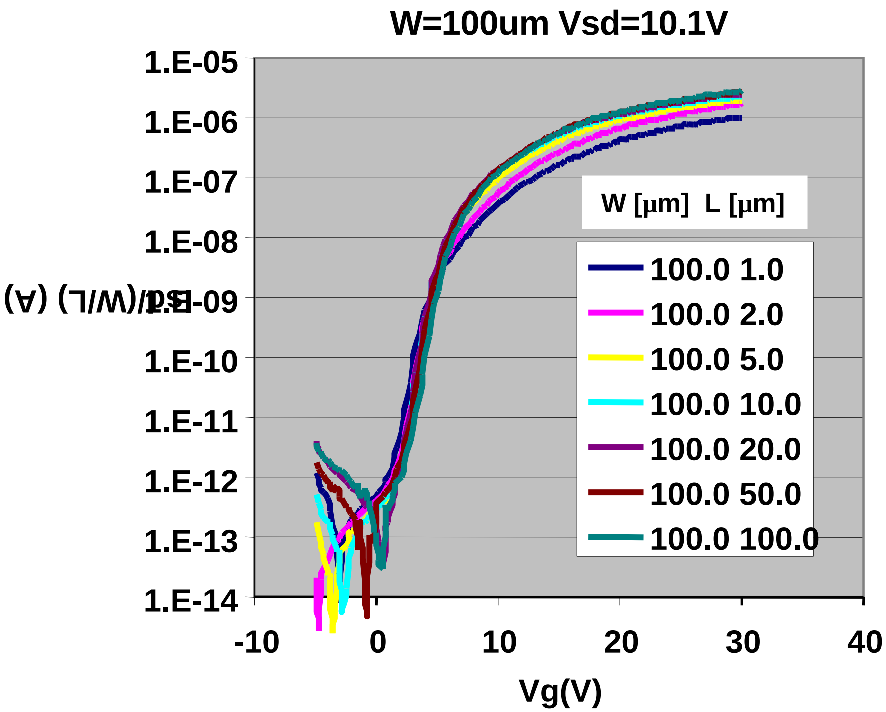
Array with data lines and TFT stack etched away to reveal how undercut has isolated the gate lines

Performance of Full-SAIL a-Si TFTs

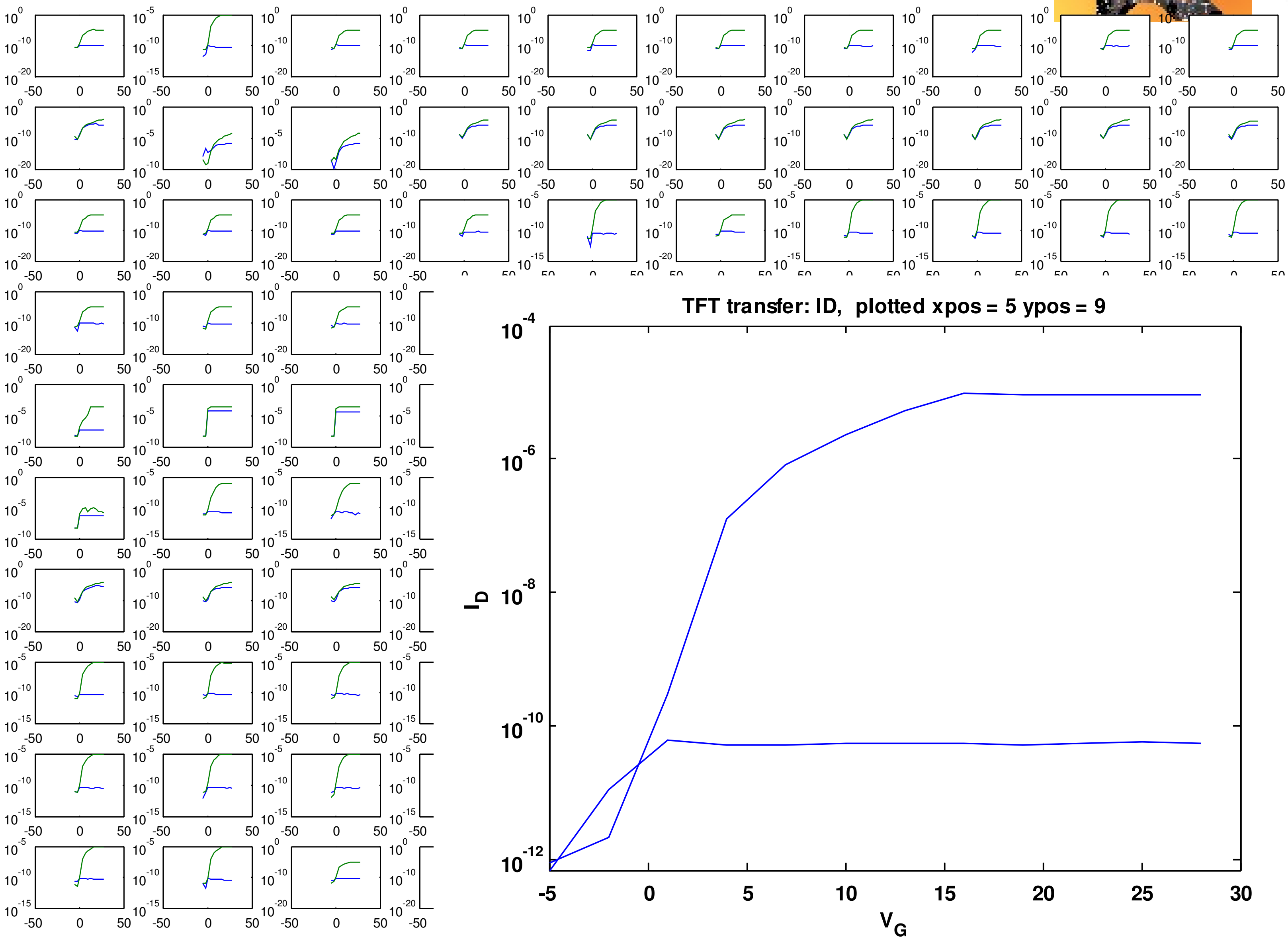
Full SAIL TFTs with thinner dielectrics have greatly improved performance

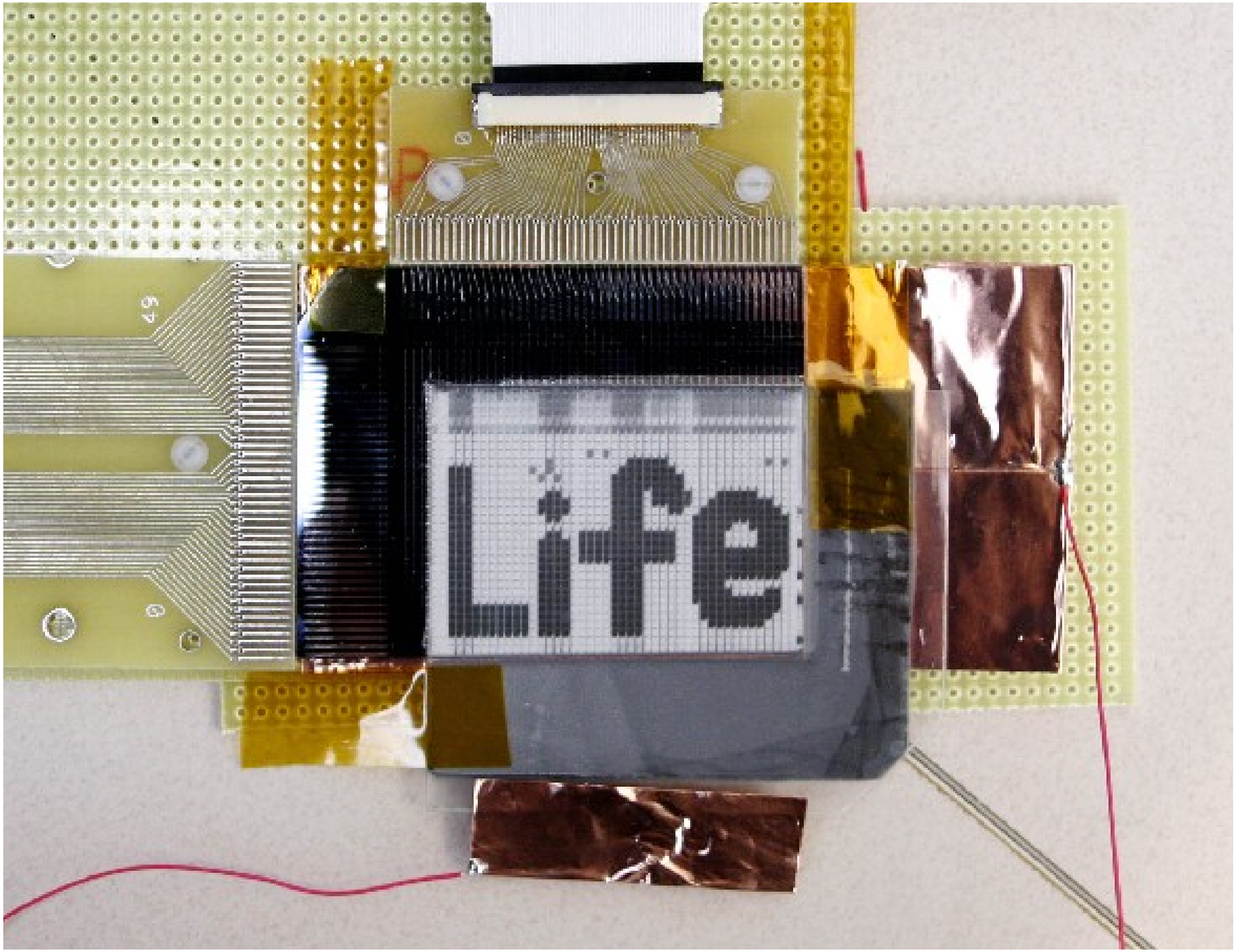
- on-off ratio > 10^7
- 100μA on-current
- mobility from linear portion of transfer curve as high as 0.8 $cm^2/V/S$
- near linear scaling of I_{on} vs 1/L to L~2μm





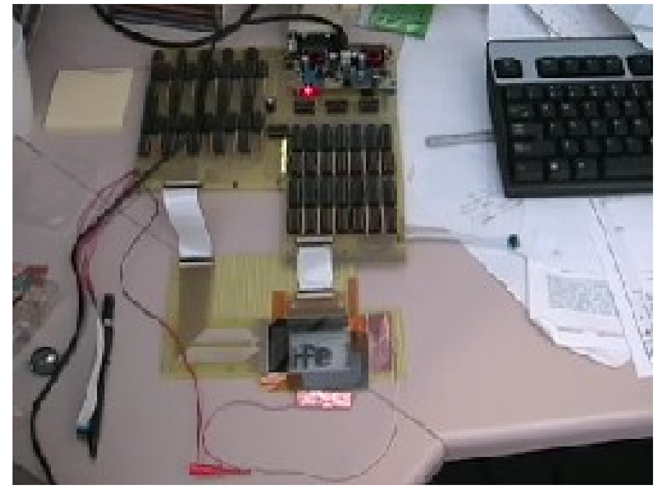
Transfer measurements on 10X10 arrays

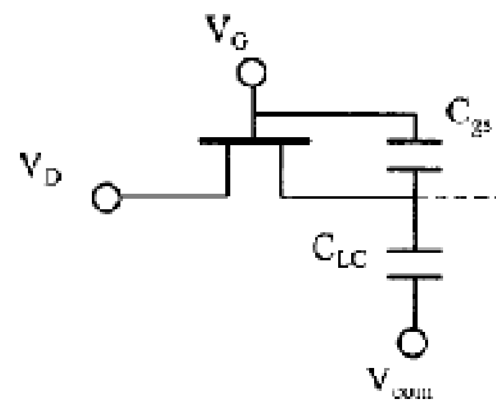



Life

Early results from the e-Ink joint venture

- Initial development on rigid substrates with proxy for SAIL process to understand electrical design issues and system integration
  - Lamination, interconnect, & pixel circuit developed
- Electrophoretic displays are pulse driven: Voltage * Time
  - Leakage must be minimized
  - High TFT on:off
  - Minimize Cgs
  - Low overlap, self aligned process is required
- Next steps: R2R SAIL demo





$$\Delta V_{LC} = \frac{C_{gs}}{C_{LC} + C_{gs}} (V_{GH} - V_{GL})$$

Summary

- R2R processing is a key enabler for high throughput & low cost production of large area AM flexible displays
- Self-Aligned Imprint Lithography (SAIL) is an end-to-end R2R process, and enables high precision interlayer alignment and resolution
- Manufacturability of SAIL TFTs and AM backplanes has been demonstrated on the plastic substrate
- TFT stack deposition and imprinting steps are achieved with R2R, and etching steps are currently in transition to the R2R environment

Acknowledgement

The authors gratefully acknowledge the support of this work through a grant from the United States Display Consortium (USDC), contract number RFP-04-112

Thank you for your Attention!