38.1: *Invited Paper:* Roll-to-Roll Fabrication of Active-Matrix Backplanes Using Self-Aligned Imprint Lithography (SAIL)

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Abstract

We have developed self-aligned imprint lithography (SAIL) technology, an innovative method for roll-to-roll (R2R) fabrication of electronic devices on flexible plastic substrates. In this paper, we present the first R2R-produced a-Si TFTs built on a polyimide substrate using the SAIL process, and prove the feasibility of this technology to enable R2R fabrication of flexible display active matrix (AM) backplanes with high precision and throughput.

1. Introduction

Inexpensive, large area arrays of thin film transistors built on flexible substrates enable many new display application opportunities that cannot be cost effectively achieved by conventional means. Recently, roll-to-roll (R2R) fabrication of electronic devices on continuous webs has attracted a great attention because it offers the possibility to significantly decrease the cost of flexible display manufacturing, especially for large sized displays.

There are a number of reasons for the lower expected cost with R2R manufacturing. Continuous steady-state processing steps are capable of eliminating the transients and latency in conventional batch processing, thereby increasing throughput and consistency. Moreover,

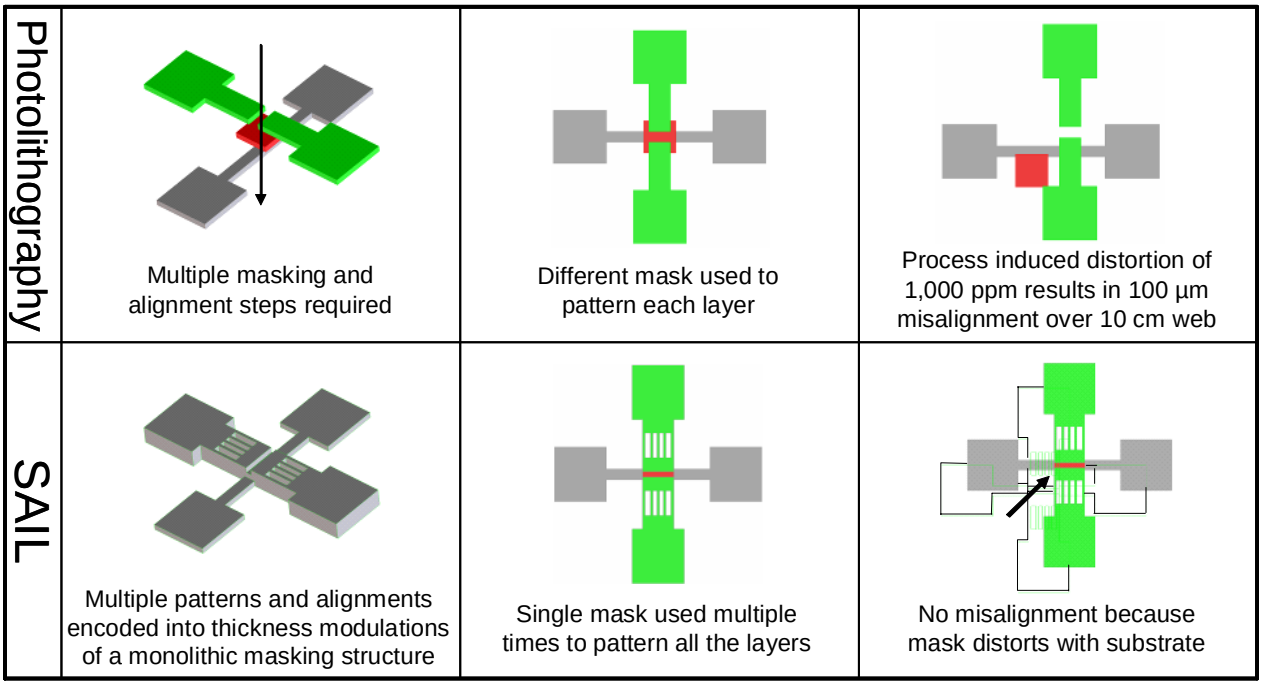


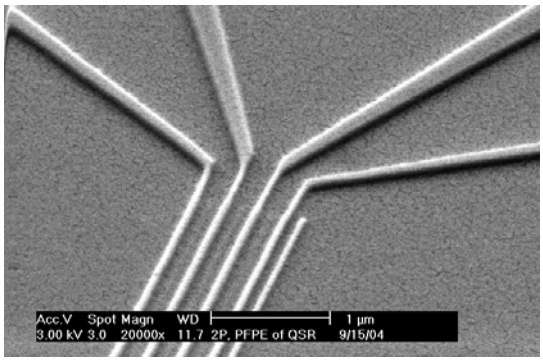
Figure 1. Schematic diagrams comparing photolithography and the SAIL process, where alignments are preserved throughout the entire processing steps because the masking structure distorts with the substrate

a rolled up web prevents any particulates from entering the devices, therefore reducing the clean room requirements. Finally, equipment costs scale with the width of the web rather than the area which for large displays becomes a significant advantage.

Despite many of its potential advantages however, flexible display manufacturing also faces a number of challenges from both business and technology standpoints. Among the crucial technological challenges is the capability to perform precision patterning and interlayer alignment.

For photolithographically patterned devices on plastic substrates, the dimensional change associated with the fabrication process can be as large as 1,000 ppm. This change translates into 100 μm of overlay misalignment if a 10 cm wide web is used. This misalignment due to dimensional instability of the substrate prevents the minimum critical feature size, such as the transistor channel length, from being smaller than the misalignment, which in this example already approaches the size of an entire pixel.

To solve this problem, we have developed R2R-based self-aligned imprint lithography (SAIL) technology, which facilitates fabrication of precision electronic devices on a large dimensionally unstable substrate by incorporating a single imprinting step. In this paper, we present the first TFTs fabricated using the SAIL process, and prove that R2R-based manufacturing of active matrix backplanes for flexible displays is feasible.



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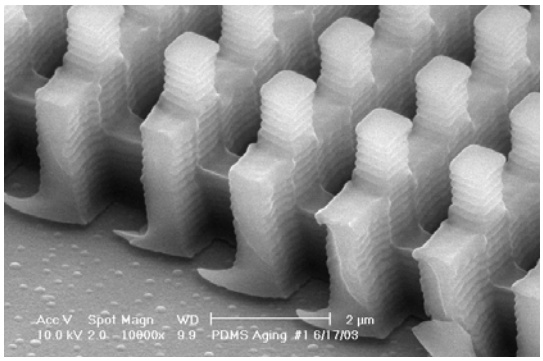


(b)

Figure 2. Scanning Electron Micrographs of R2R imprinted structures; (a) a 40nm wide line array; (b) an array of sub-micron features with four levels and 5:1 aspect ratio

2. SAIL process

In the SAIL process, all the geometric information needed to pattern each layer of an active matrix backplane is contained in a monolithic, multi-level 3-D mask that is imprinted on top of the device materials deposited on the substrate. Each level of the mask contains information about different masking levels. Since this pre-aligned masking structure distorts with the substrate whenever a dimensional change occurs, critical interlayer alignments, such as the source and drain (S/D) overlap of the gate, are preserved throughout the entire processing steps. Figure 1 illustrates this unique and important characteristic of the SAIL process, and compares it with the photolithographic process when a noticeable amount of substrate distortion is introduced.

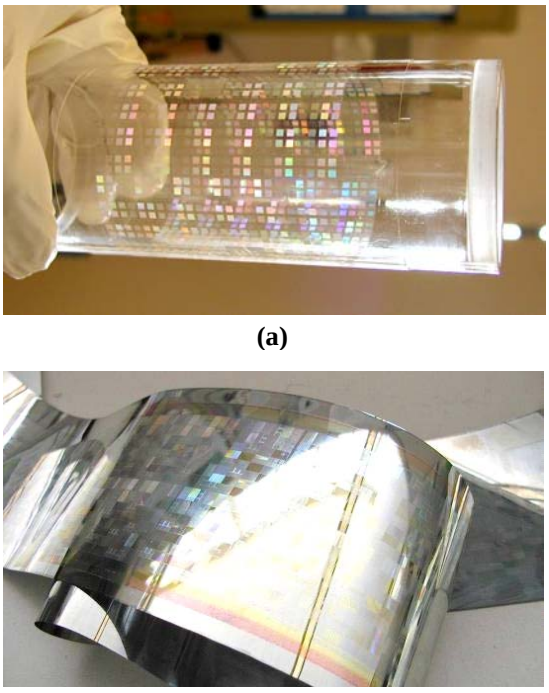
2.1 Deposition

In our process, all of the TFT materials are deposited before any patterning is performed. This approach is well suited to an inline sequential R2R deposition system. Inline deposition of the full TFT stack has advantages of avoiding contamination of critical interfaces, minimizing the footprint of the deposition equipment, and relaxing the clean room requirements for subsequent processes. For our TFT structures, the thin film stack was deposited on a thin polyimide web using the production R2R deposition system. The complete material stack consists of a gate metal, a bilayer dielectric of SiN_x and SiO_2, an amorphous Si, an n+ microcrystalline Si, and finally, a source and drain contact metal. The highest processing temperature is 250 ºC, and the deposition processes are identical whether the stack will be used to produce TFTs by the SAIL or photolithography process.

2.2 Imprinting

Imprint lithography differs from photolithography in that instead of using a sequential series of etch masks, the complete pattern is transferred to the masking material in an single step by molding it with a compliant stamp. The result is a multi-level mask, where each level of the mask corresponds to the pattern produced by one alignment and exposure step in traditional photolithography. In the SAIL process, the thickness modulation of a monolithic pre-aligned multi-level mask enables patterning of a multiple number of layers because each level of the mask contains the layout information for each TFT stack layer. Uniformly thinning down the entire mask structure one level at a time uncovers the device layer to be patterned in the next process step.

Because there is only one imprinting step involved, this process is highly suitable for R2R manufacturing. A major advantage of the SAIL process is its ability to create aligned high resolution structures with a high throughput R2R process. Figure 2 shows scanning electron micrographs of 40 nm wide lines and sub-micron scale 5:1 aspect ratio features imprinted at a throughput rate of 5 m/min using the R2R imprinting machine we have developed. Sub-micron scale patterning capability has a benefit for display manufacturing because with constant switching voltage the pixel speed depends linearly on mobility but inversely with the square of channel length so that short channel length devices enable fast response even with a lower mobility material system. The high aspect ratio capability is a prerequisite to make a mask structure with a large number of levels and complex geometry. A R2R stamp roller and the resulting continuous web with patterns imprinted are shown in Figure 3.



(a) **(b)**

Figure 3. R2R imprint stamp and the resulting web; (a) an imprinting roller used for R2R imprinting process; (b) continuous web with patterns imprinted with a R2R process

2.3 Self-Aligned Etch

Once a pre-aligned 3-D mask is imprinted on top of the TFT stack, a series of selective etches are applied to the mask and the device materials to pattern each layer, thereby fabricating the TFT devices. Figure 4 (a) shows a schematic diagram illustrating that a pre-aligned multi-level mask is imprinted on top of the TFT stack. Figure 4 (b)

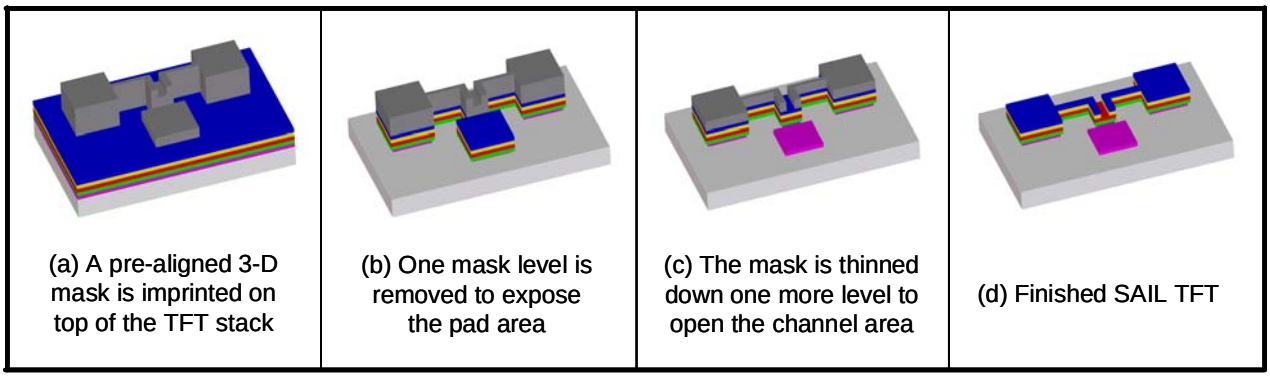


Figure 4. Schematic diagrams illustrating a process flow for SAIL TFT fabrication

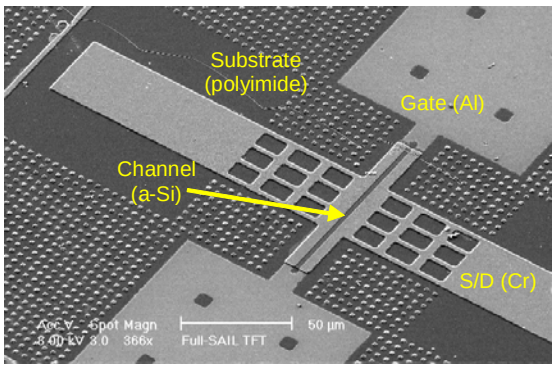
shows that the entire mask structure level is uniformly thinned down to expose the pad area, followed by another level removal step opening up the channel area as shown in Figure 4 (c). In these steps, TFT stack etch steps are followed by the mask etch steps in an alternating way. All etches are mutually selective. After etching the n+ layer and removing the remaining mask material, the SAIL TFT fabrication is finished as shown in Figure 4 (d). All the required alignment information is already provided with the mask structure so that the subsequent etch steps are performed in a self-aligned manner, one of the distinguishing features of the SAIL process.

The resulting devices are shown in Figure 5. Figure 5 (a) shows an individual bottom gate TFT device fabricated on a polyimide substrate using the SAIL process. Figure 5 (b) shows a part of the 10x10 SAIL TFT arrays currently under fabrication.

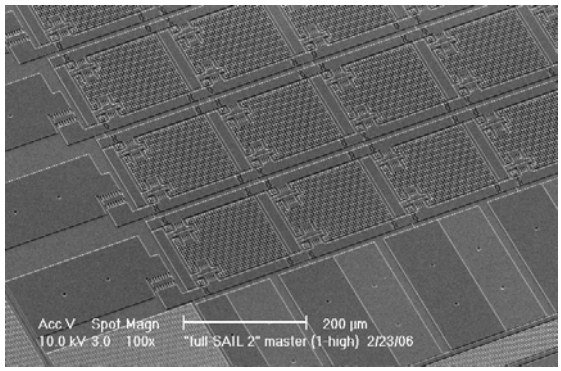
The SAIL TFT devices we present in this paper were etched in a batch mode, unlike the deposition and imprinting steps done by means of R2R processes. Recently, we have built a R2R reactive ion etcher (RIE) system, and the etch processes developed in batch modes are being transitioned to the R2R manufacturing environment, making the process an end-to-end R2R one.

3. SAIL TFTs

Figure 6 shows the output and gate leakage characteristics of the SAIL TFTs. The first set of plots in Figure 6 (a) was obtained from continuous gate TFTs with W/L=100/100 μm, whereas the second set in Figure 6 (b) is from isolated TFT devices with W/L=50/1 μm. Comparing the two types of devices, it is noted that the isolated gate TFTs show significantly less leakage than the continuous gate TFTs due to the reduction in the overlap of the gate by the source and drain contacts. However, the isolated TFTs with 1 μm channel length exhibit short channel effect where the barrier between source and drain is no longer large enough to prevent current between the source and drain particularly for large V_{sd}. This effect is an example of the issues related to the high resolution capability of SAIL. Another issue is that as channel length decreases the contact resistance becomes more significant than the channel resistance and the S/D current stops inversely scaling with channel length. Work is in progress to overcome the stated problems and improve the resulting performance.



(a)



(b)

Figure 5. Scanning electron micrographs of the SAIL TFT devices; (a) an individual TFT; (b) a 10x10 SAIL TFT array

Finally, having demonstrated individual devices, we are working to make 10x10 TFT arrays using the SAIL process. Integrated with a frontplane, these arrays will be used as AM backplanes of a prototype R2R-manufactured flexible display.

4. Conclusion

We have developed the SAIL process and proved its feasibility to fabricate functioning TFTs on a plastic substrate. This self-aligned process is designed to be fully R2R compatible by combining multiple patterning and alignment steps of photolithography into thickness modulations of a pre-aligned monolithic 3-D mask and performing an alternating series of mutually selective etches on the mask and device layers. The SAIL process enables precision patterning and interlayer alignment on dimensionally unstable flexible substrates. As a result, this process is suitable for R2R-based manufacturing of high precision flexible display AM backplanes at high throughput. The high resolution of the SAIL process brings up issues related to small features and high performance. Currently, deposition and imprinting steps are

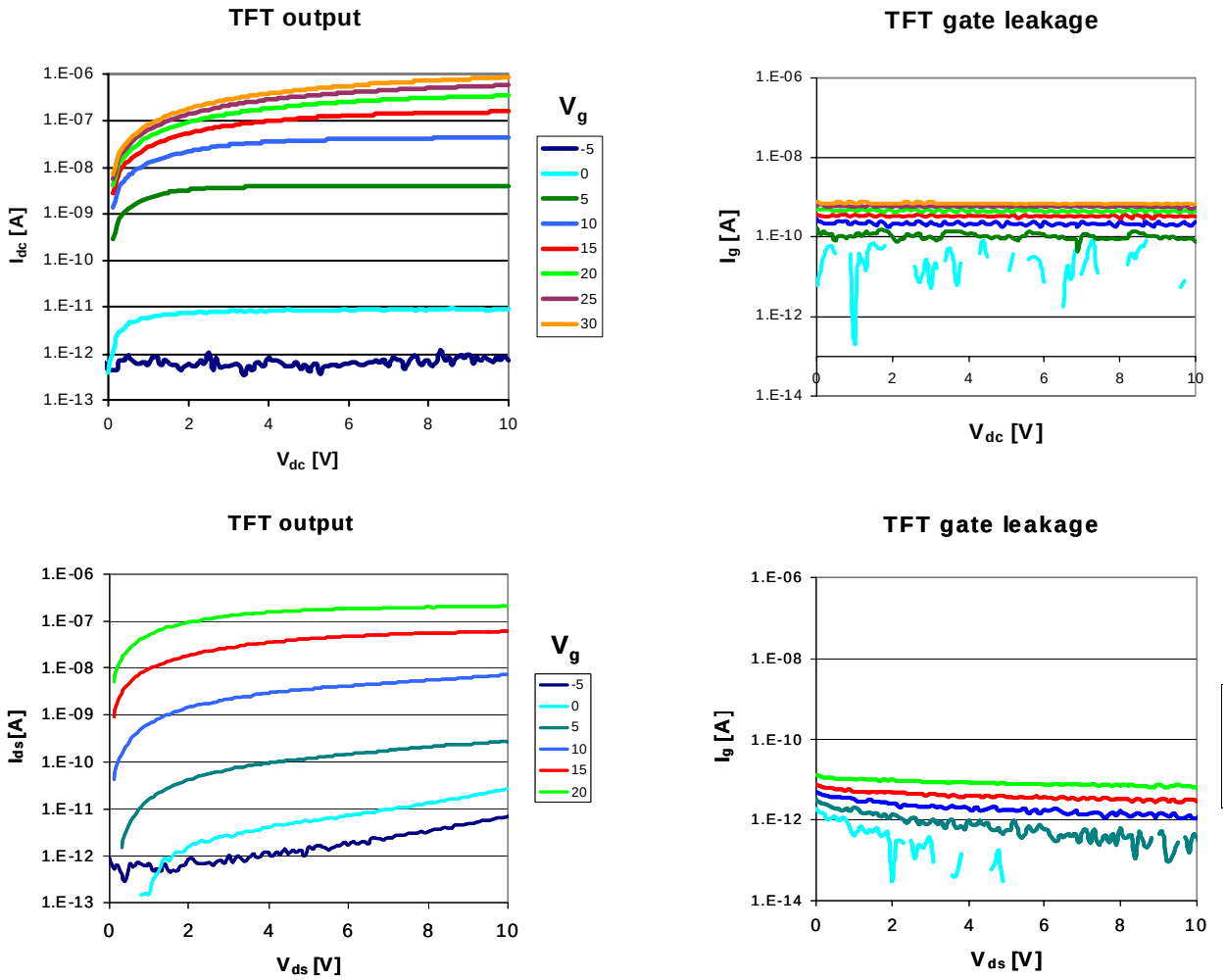


Figure 6. Output and gate leakage measured from SAIL TFTs; (a) continuous gate TFTs (L=100 µm); (b) isolated gate TFTs (L=1 µm)

fully R2R compatible, while etching steps are being transitioned from the batch mode to the R2R environment. Work is underway to fabricate SAIL TFT arrays for a prototype display demonstration and to improve the basic process and device performance.

5. Acknowledgements

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6. References

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